1 TABLE OF CONTENTS

2 REVISION HISTORY

Revision	Description	Issue Date
Rev. 0.1	Initial Issued	May.06.2016
Rev. 0.2	Revised typos	May.19.2016
Rev. 0.3	Revised the address bit length from 32 bits to 24 bits	Oct.13.2016
Rev. 0.4	Added ***Command Termination*** in page 7 Revised ***Truth Table*** in page 7	May.03.2017

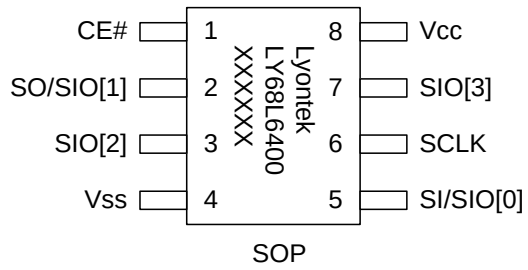
3 FEATURES

- 50Ω Output Drive Strength LVCMOS.
- 1K or 32 byte wrapped burst length via toggle command.
- Linear Burst with Row Boundary Crossing (RBX) is supported up to 84MHz.
- **Green package available**
- Package : 8-pin 150mil SOP

4 SPECIFICATIONS

- Single Supply Voltage:
  - V_{CC}=2.7 to 3.6V
  - V_{CCQ}=2.7 to 3.6V
- Interface: SPI/QPI with SDR mode
- Performance: Clock rate up to 100MHz
- Organization: 64Mb, 8M x 8bits with 1,024 byte page size
  - Column address: AY0 to AY9
  - Row address: AX0 to AX12
- Refresh: Self-managed
- Operating temperature range
  - TC = -25°C to +85°C
- Maximum Standby Current:
  - 400µA @ 85°C

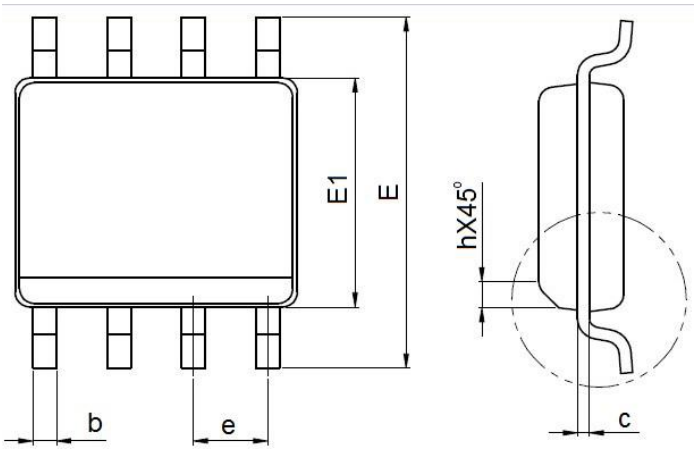
5 PIN CONFIGURATION

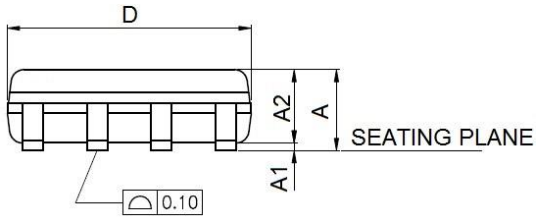


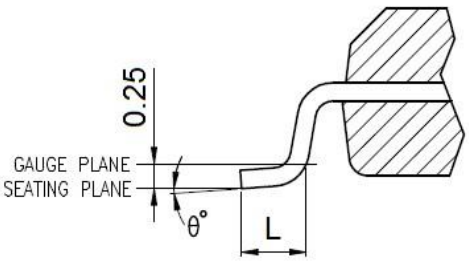
SOP

6 PACKAGE OUTLINE DIMENSION

8-pin 150mil SOP Package Outline Dimension







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	STANDARD	
	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

NOTES:

1. JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
   MS-012 BA REV.F (THERMAL)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

7 ORDERING INFORMATION

Table 1: Ordering Information

Package Type	Maximum Clock Rate(MHz)	Temperature Range(℃)	Packing Type	Lyontek Item No.
8-pin (150mil) SOP	100	-25℃~85℃	Tube	LY68L6400SL
			Tape Reel	LY68L6400SLT

8 PIN DESCRIPTION

Table 2: Signals Table

SYMBOL	TYPE	SPI Mode Function	QPI Mode Function	COMMENTS
V_{CC}	Power	Core supply 3V		
V_{SS}	Ground	Core supply ground		
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state.		
CLK	Input	Clock Signal		
SI/SIO[0]	I/O	Serial Input	I/O[0]	
SO/SIO[1]	I/O	Serial Output	I/O[1]	
SIO[2]	I/O	-	I/O[2]	
SIO[3]	I/O	-	I/O[3]	

9 POWER-UP INITIALIZATION

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When V_{CC} reaches a stable level at or above minimum V_{CC}, the device will require 150µs and user-issued RESET Operation (see section 12) to complete its self-initialization process. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track V_{CC} within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the 150µs period the device is ready for normal operation.

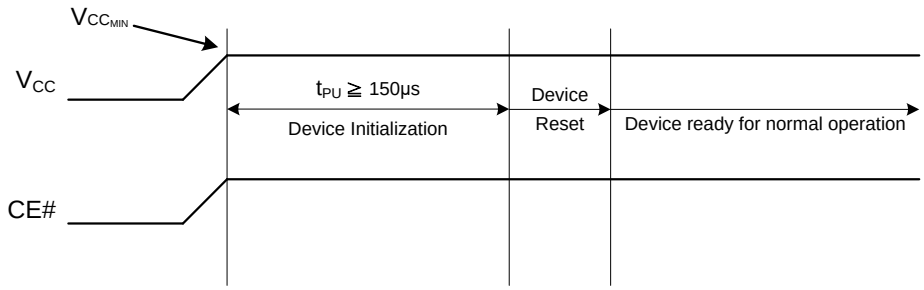


Figure 1 : Power-Up Initialization Timing

10 INTERFACE DESCRIPTION

10.1 Address Space

SPI/QPI PSRAM device is byte-addressable. 64M device is addressed with A[22:0].

10.2 Page Length

Read and write operations are always in wrap mode within 1K bytes. Linear Burst with Row Boundary Crossing (RBX) available as long as t_{CEM} is met.

10.3 Drive Strength

The device powers up in 1/2 strength (50Ω).

10.4 Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

10.5 Truth Table

The device recognizes the following commands specified by the various input methods.

COMMAND	CODE	SPI Mode (QE=0)					QPI Mode (QE=1)				
		CMD	Addr	Wait Cycle	DIO	MAX. Freq.	CMD	Addr	Wait Cycle	DIO	MAX. Freq.
Read	‘h03	S	S	0	S	33	N/A				
Fast Read	‘h0B	S	S	8	S	100	Q	Q	4	Q	66
Fast Read Quad	‘hEB	S	Q	6	Q	100	Q	Q	6	Q	100*
Write	‘h02	S	S	0	S	100	Q	Q	0	Q	100*
Quad Write	‘h38	S	Q	0	Q	100	Same as ‘h02				
Enter Quad Mode	‘h35	S	-	-	-	100	N/A				
Exit Quad Mode	‘hF5	N/A					Q	-	-	-	100
Reset Enable	‘h66	S	-	-	-	100	Q	-	-	-	100
Reset	‘h99	S	-	-	-	100	Q	-	-	-	100
Set Burst Length	‘hC0	S	-	-	-	100	Q	-	-	-	100
Read ID	‘h9F	S	S	0	S	100	N/A				

Remarks: S = Serial I/O, Q = Quad I/O

*Quad operations that cross a row boundary are limited to 84 MHz MAX.

10.6 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active read/write wordline and set the device into standby. Not doing so will block internal refresh operations until the device sees the read/write wordline terminated.

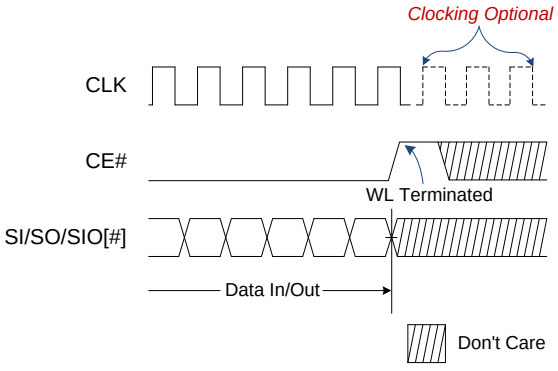


Figure 2 : Command Termination

11 SPI MODE OPERATIONS

The device powers up into SPI mode by default but can also be switched into QPI mode.

11.1 SPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

SPI Reads can be done in three ways:

1. 'h03: Serial CMD, Serial I/O, slow frequency
2. 'h0B: Serial CMD, Serial I/O, fast frequency
3. 'hEB: Serial CMD, Quad I/O, fast frequency

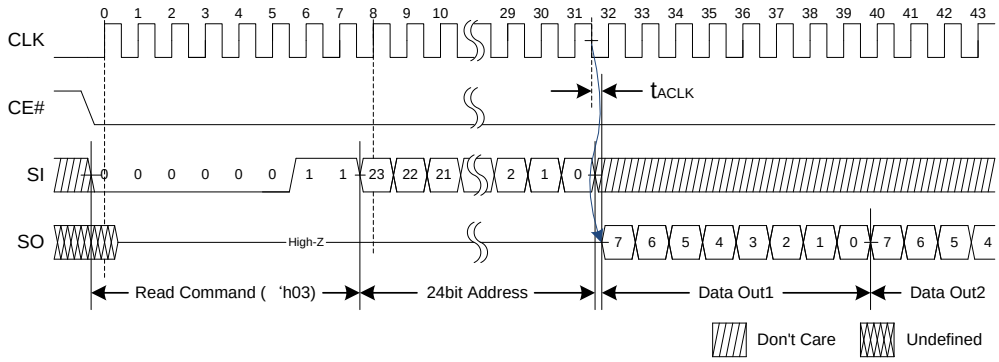


Figure 3 : SPI Read 'h03 (MAX. freq. 33MHz)

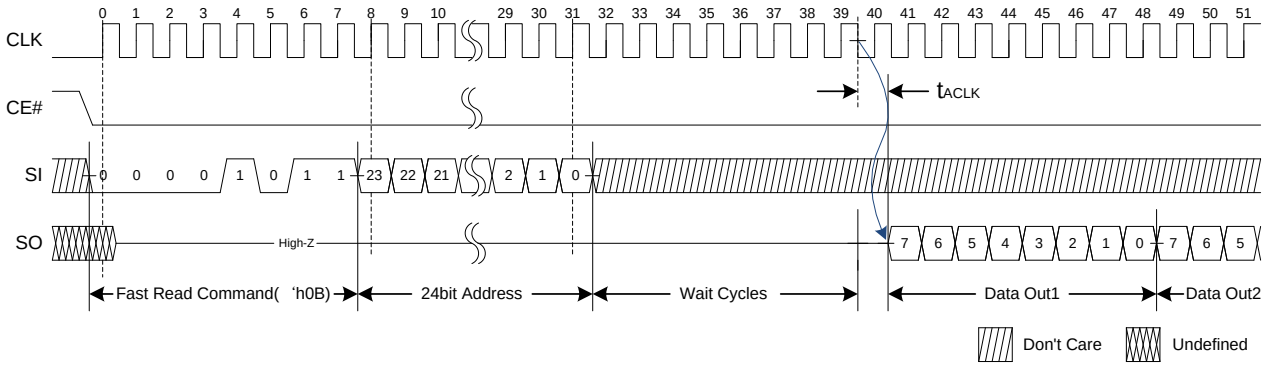


Figure 4 : SPI Fast Read 'h0B (MAX. freq. 100MHz)

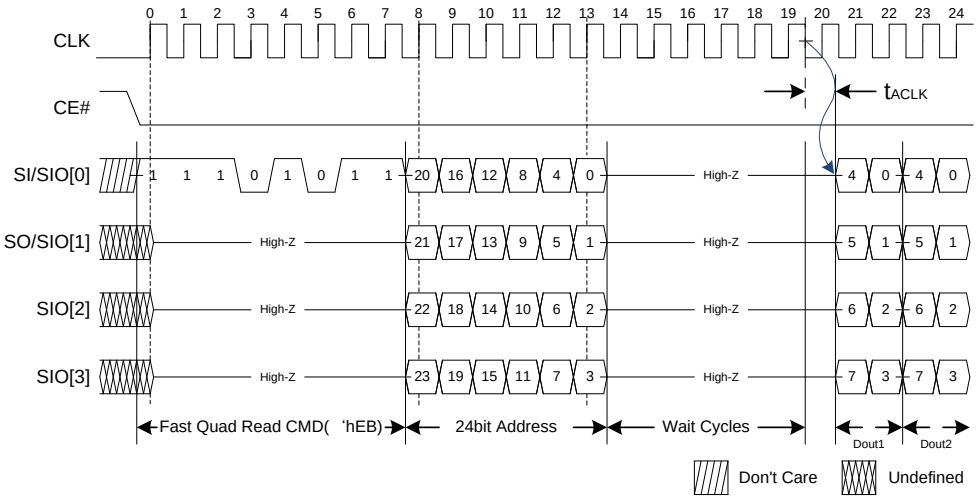


Figure 5 : SPI Fast Quad Read 'hEB (MAX. freq. 100MHz)

11.2 SPI Write Operations

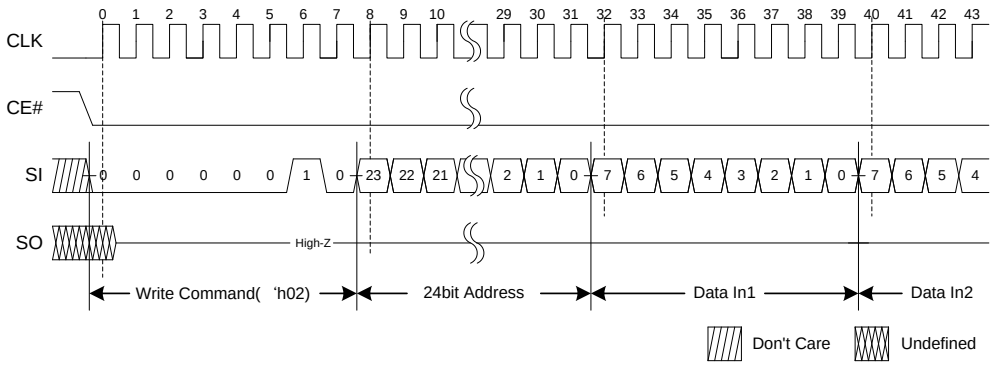


Figure 6 : SPI Write 'h02

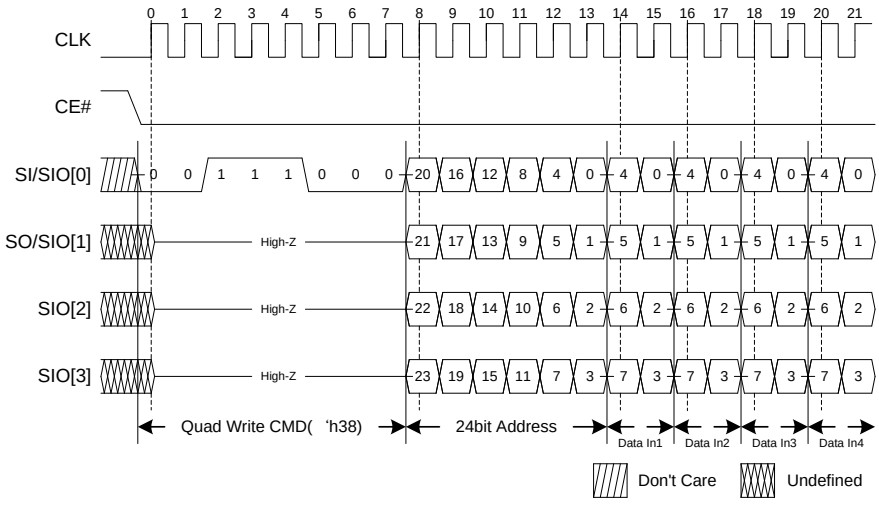


Figure 7 : SPI Quad Write 'h38

11.3 SPI Quad Mode Enable Operation

This command switches the device into quad I/O mode.

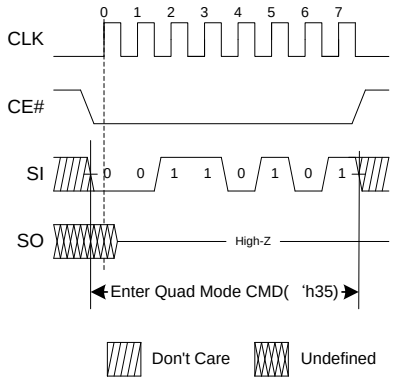


Figure 8 : Quad Mode Enable 'h35 (available only in SPI mode)

11.4 SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

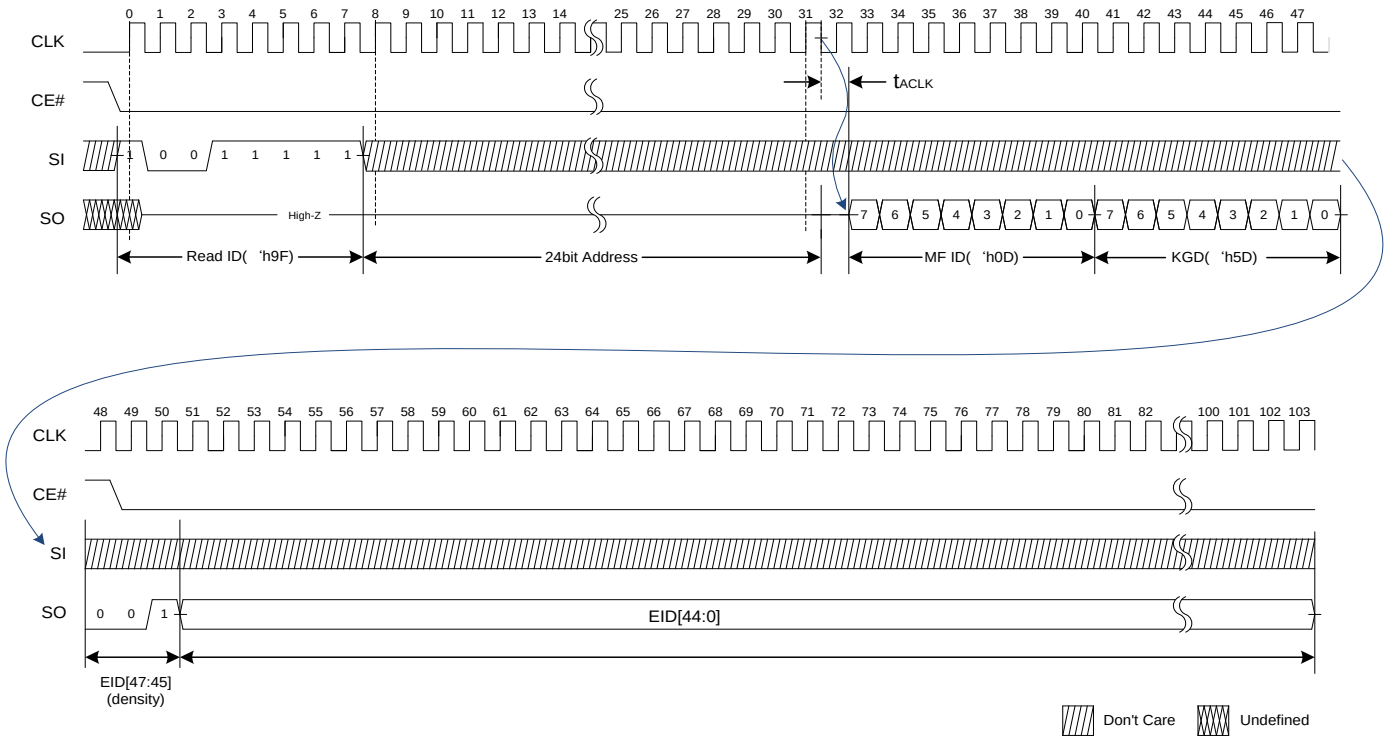


Figure 9 : SPI Read ID 'h9F (available only in SPI mode)

Table 3: Known Good Die (KGD)

KGD[7:0]	Known Good Die
'b0101_0101	FAIL
'b0101_1101	PASS

*Note: Default is FAIL die, and only mark PASS after all tests passed.

12 QPI MODE OPERATIONS

12.1 QPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

QPI Reads can be done in one of two ways:

1. 'h0B: Quad CMD, Quad I/O, slow frequency
2. 'hEB: Quad CMD, Quad I/O, fast frequency

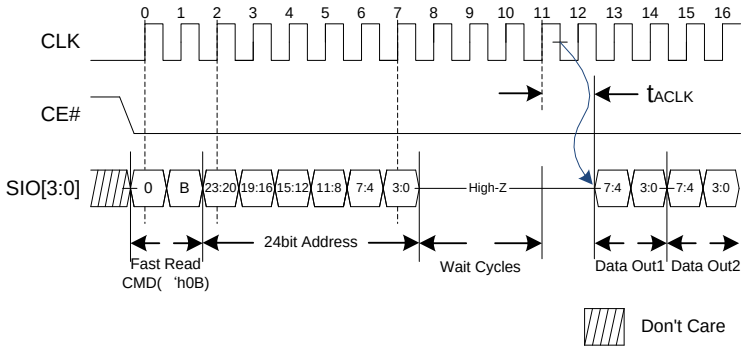


Figure 10 : QPI Fast Read 'h0B (MAX. freq. 84MHz)

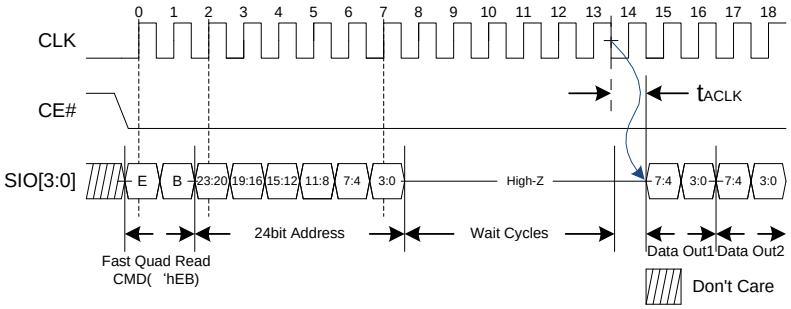


Figure 11 : QPI Fast Quad Read 'hEB (MAX. freq. 100MHz)

12.2 QPI Write Operation(s)

QPI write command can be input as ‘h02 or ‘h38.

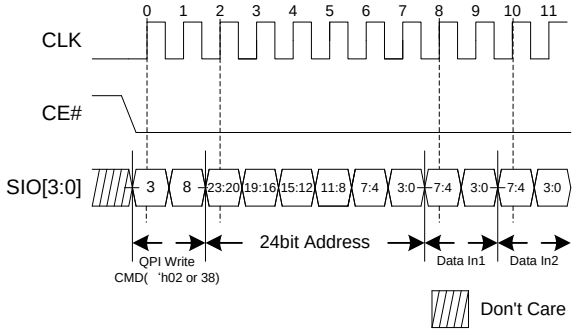


Figure 12 : QPI Write ‘h02 or ‘h38

12.3 QPI Quad Mode Exit Operation

This command will switch the device back into serial I/O mode.

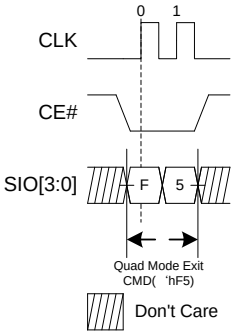


Figure 13 : Quad Mode Exit ‘hF5
(only available in QPI mode)

13 RESET OPERATION

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

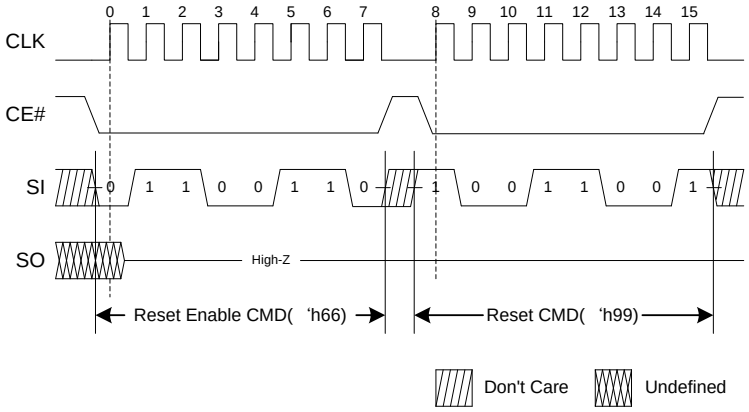


Figure 14 : SPI Reset

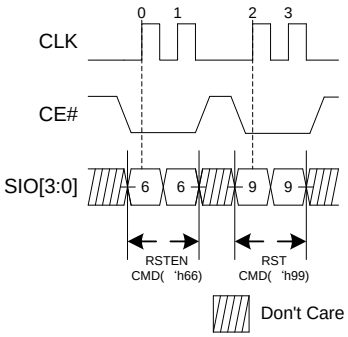


Figure 15 : QPI Reset

The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable procedure.

14 SET BURST LENGTH OPERATION

The Set Burst Length Operation toggles the device's burst length wrap between 1024 and 32. Default burst length is 1024. This command has no effect on RBX Enabled parts.

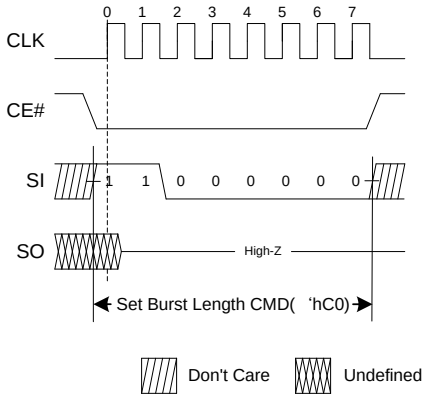


Figure 16 : SPI Set Burst Length 'hC0

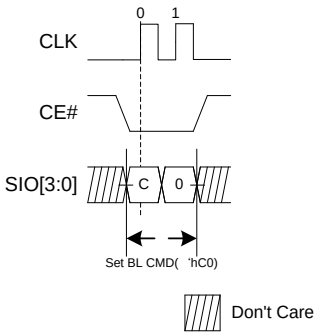


Figure 17 : QPI Set Burst Length 'hC0

15 INPUT / OUTPUT TIMING

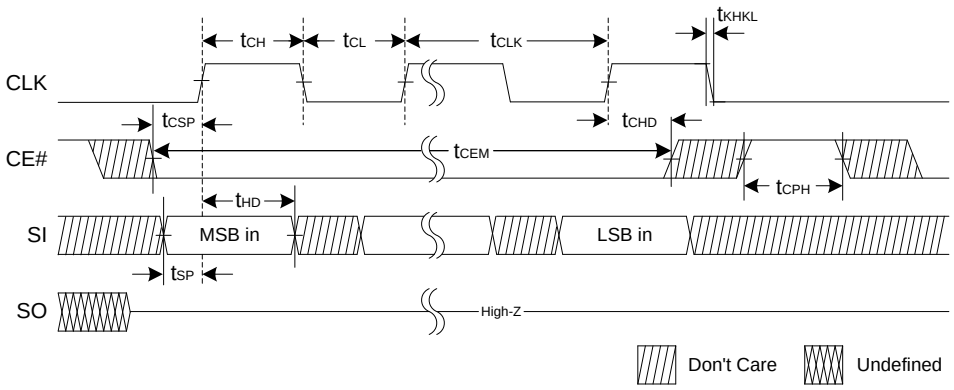


Figure 18 : Input Timing

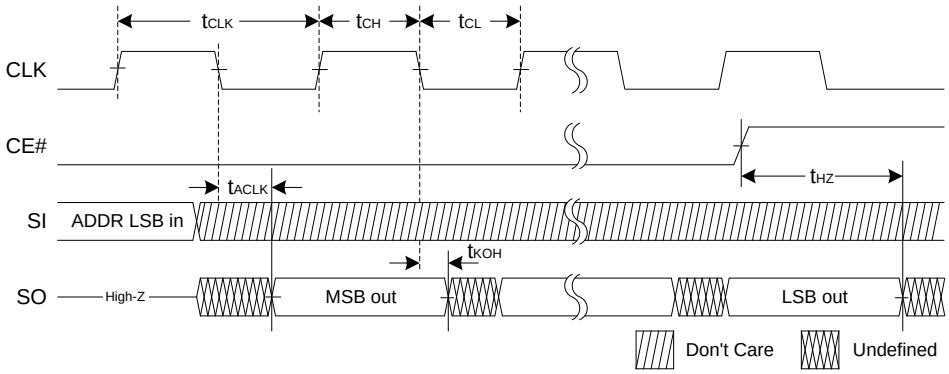


Figure 19 : Output Timing

16 ELECTRICAL SPECIFICATIONS

16.1 Absolute Maximum Ratings*

Table 4: Absolute Maximum Ratings*

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Voltage to any pad except V_{CC} relative to V_{SS}	VT	-0.3 to V_{CC} +0.3	V	
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.2 to +4.2	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Note: 1. Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

* Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

16.2 Operating Conditions

Table 5: Operating Characteristics

PARAMETER	MIN.	MAX.	UNIT
Operating Temperature	-25	85	°C

16.3 DC Electrical Characteristics

Table 6: DC Characteristics

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	2.7	3.6	V	
V_{IH}	Input high voltage	V_{CC}-0.4	V_{CC}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{CC}	-	V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)	-	0.2 V_{CC}	V	
I_{LI}	Input leakage current	-	1	µA	
I_{LO}	Output leakage current	-	1	µA	
I_{CC}	Read/Write	-	40	mA	
I_{SB}	Standby current @ 85°C	-	400	µA	

16.3 AC Electrical Characteristics

Table 7: READ/WRITE Timing

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{CLK}	CLK period - SPI Read('h03)	30.3	-	ns	33MHz
	CLK period - QPI Fast Read('h0B)	11.9	-		84MHz
	CLK period – all other operations	9.6	-		100MHz
t_{CH} / t_{CL}	Clock high/low width	0.45	-	t_{CLK}(min)	
t_{KHKL}	CLK rise or fall time	-	1.5	ns	
t_{CPH}	CE# HIGH between subsequent burst operations	9.6	-	ns	
t_{CEM}	CE# low pulse width	-	2	µs	
t_{CSP}	CE# setup time to CLK rising edge	3	-	ns	
t_{CHD}	CE# hold time from CLK rising edge	3	-	ns	
t_{SP}	Setup time to active CLK edge	2.5	-	ns	
t_{HD}	Hold time from active CLK edge	2	-	ns	
t_{HZ}	Chip disable to DQ output high-Z	-	7	ns	
t_{ACLK}	CLK to output delay	-	7	ns	
t_{KOH}	Data hold time from clock falling edge	1.5	-	ns	

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