SiI9678 HDMI Transmitter with HDCP 2.2

Support

Data Sheet

SiI-DS-1142-B

April 2014

Contents

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Tables

1. General Description

The SiI9678 HDMI® transmitter is a High Definition Multimedia Interface (HDMI) transmitter. This transmitter supports HDMI 1.4 Specification on a wide range of BD/STB products.

The SiI9678 transmitter supports up to 4K x 2K video mat.

The SiI9678 transmitter supports High-bandwidth Digital Content Protection (HDCP) 2.2 Specification devices that require secure content delivery.

1.1. HDMI Input

- Supports 24/30/36-bit RGB/YCbCr 4:4:4/xvYCC, and 16/20/24-bit YCbCr 4:2:2 video input mats.
- Supports video mat up to 4K x 2K @ 30 Hz RGB/YCbCr 4:4:4/YCbCr 4:2:2, and supports up to 4K x 2K @ 60Hz YCbCr 4:2:0.
- Supports 3D video mat up to 1080p @ 60 Hz.
- Supports high resolution VESA mode video mat up to QSXGA @ 60 Hz.
- Support HDCP 1.4.
- Low power 1.0 V core.

1.2. HDMI Output

- Supports HDCP 1.4 and HDCP 2.2.
- HDMI and DVI compatibility.
- HDMI Type A, Type C, and micro-D connector support.

1.3. Features

- Supports HDMI 1.4 Specification.
- Supports HDCP 1.4/2.2 Specification.
- Supports color space conversions among RGB, YCbCr 4:4:4 and YCbCr 4:2:2 video mats without deep color.
- Supports color space conversions between RGB and xvYCC video mats without deep color.

1.4. Packaging

- 76-pin QFN (9 mm × 9 mm) package
- Standard part covers extended (–20 °C to +85 °C) temperature range

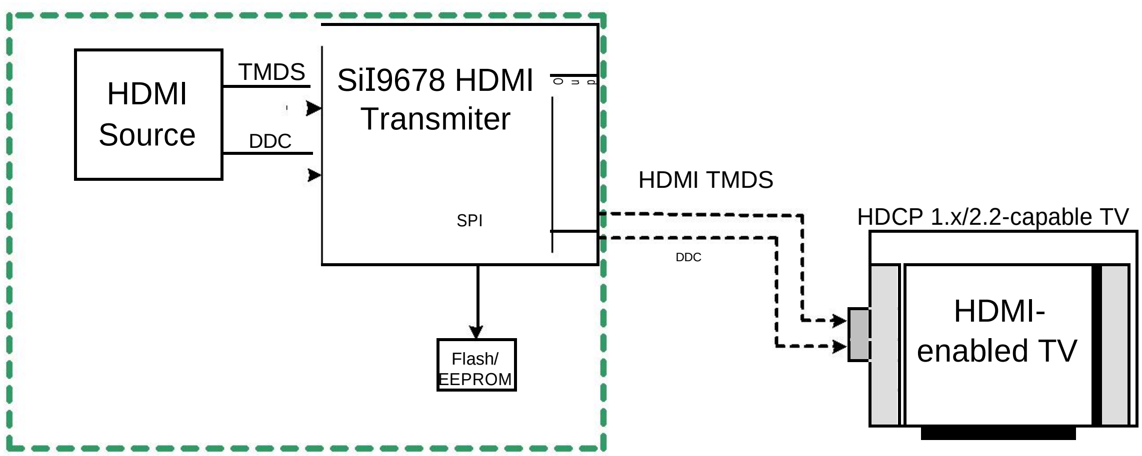


Figure 1.1. Typical Application (SiI9678 HDMI Transmitter)

1.5. Pin Diagram

Figure 1.2 shows the pin assignments of the SiI9678 transmitter. Refer to the Pin Descriptions section beginning on page 21 describes the pin functions. The SiI9678 device is a 76-pin 9 mm × 9 mm QFN package with ePad, which ***must*** be connected to ground.

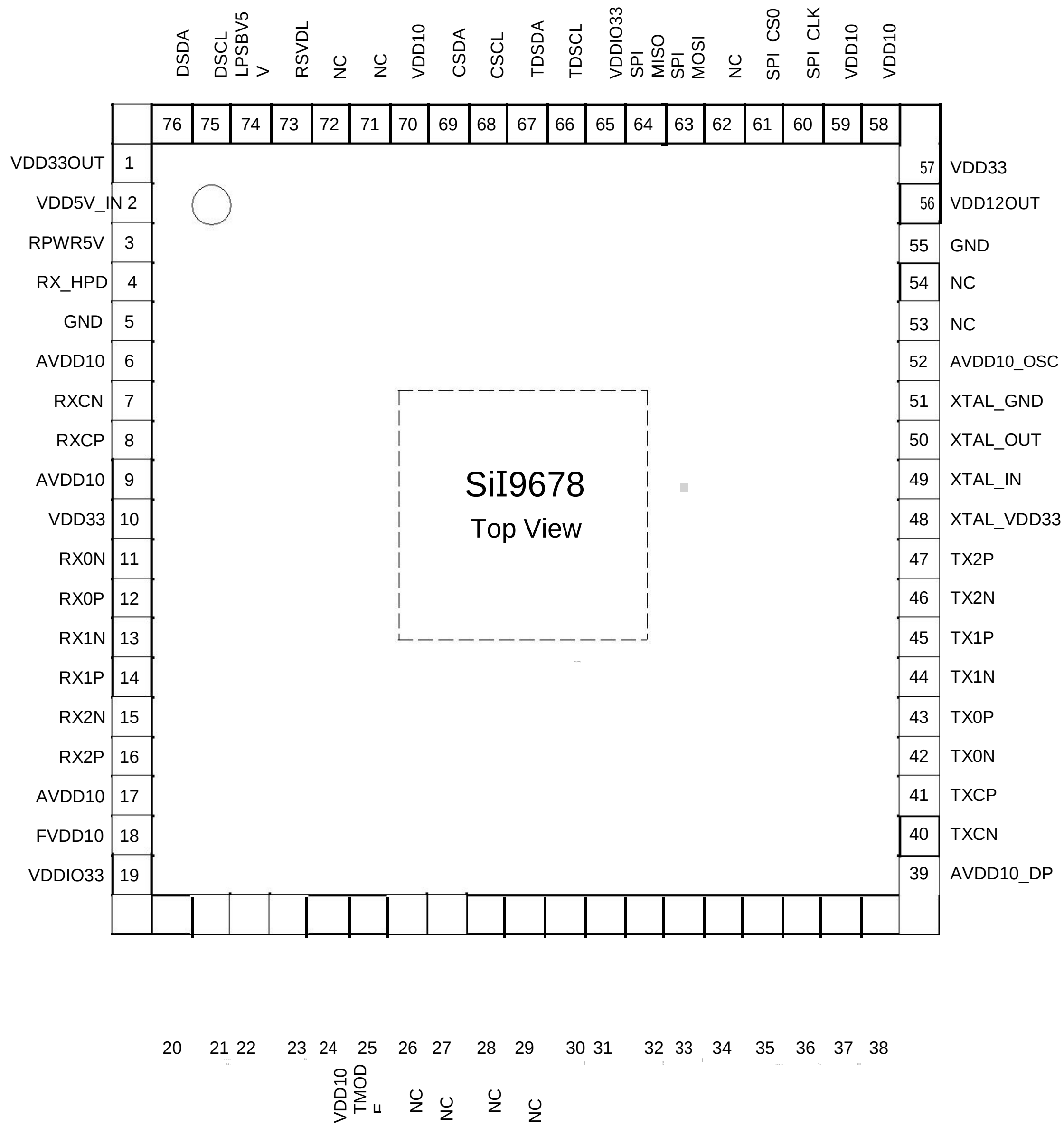


Figure 1.2. Pin Diagram (Top View)

2. Functional Description

The SiI9678 HDMI transmitter provides a complete solution transmitting ultra-high resolution (such as WQXGA, QSXGA, and 4K x 2K) with HDCP encryption. The SiI9678 transmitter can support HDMI output with HDCP 1.4 encryption or HDCP 2.2 encryption. Figure 2.1 shows the functional block diagram of the SiI9678 transmitter.

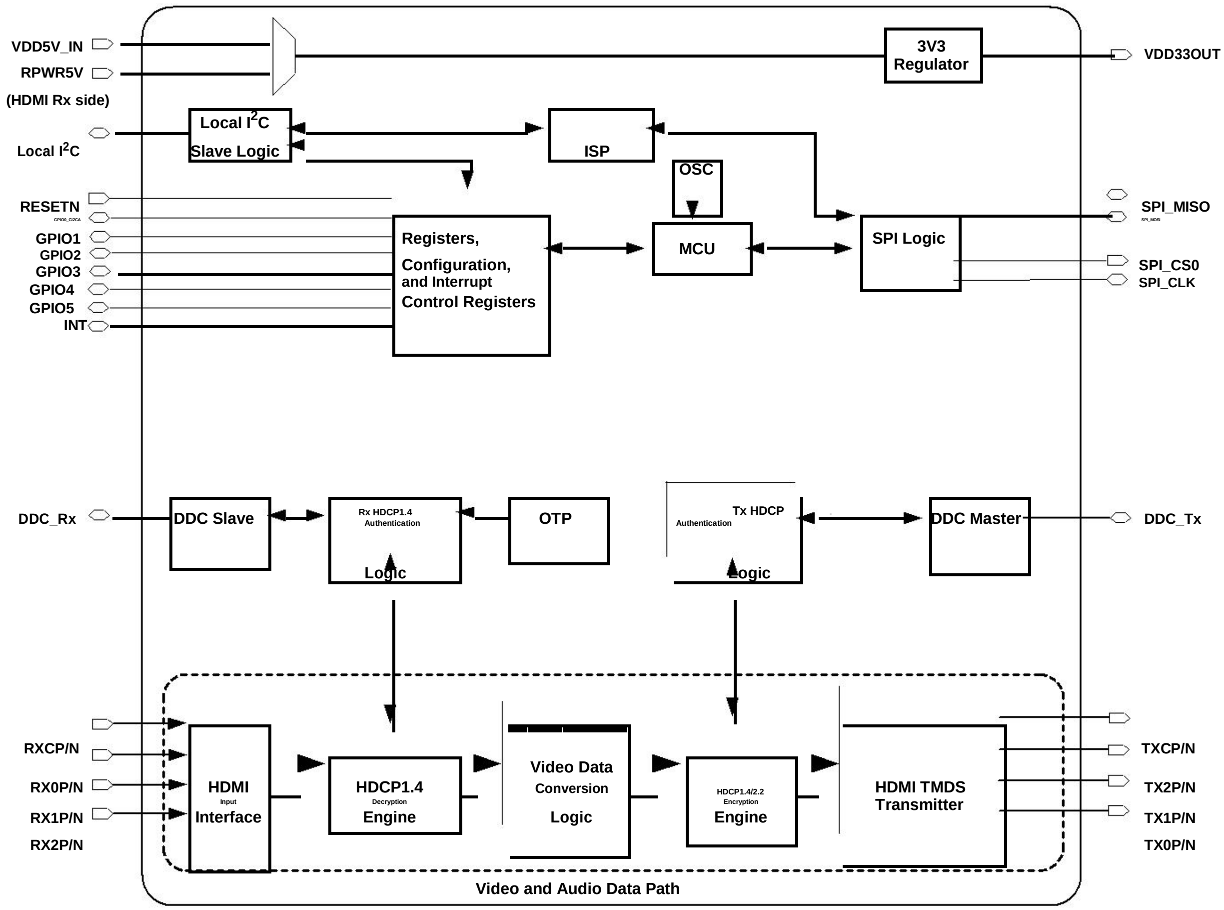


Figure 2.1. Functional Block Diagram

The SiI9678 HDMI transmitter provides an HDMI input interface. This interface supports TMDS clock speed up to 300 MHz. Refer to Table 2.1 supported 2D video mats. See the 3D Video mats section on page 26 the details of the supported 3D mats.

Table 2.1. Supported 2D Video mats

2D Video Resolution	Pixel mat	Bus Width	Maximum Frame Rate (Hz)
VGA	RGB	24	60
WVGA	RGB	24	60
SVGA	RGB	24	60
XGA	RGB	24	60
SXGA	RGB	24	60
UXGA	RGB	24	60
WUXGA	RGB	24	60
QXGA	RGB	24	60
WQXGA	RGB	24	60
480p/i	RGB YCbCr 4:4:4	24, 30, 36	60
	YCbCr 4:2:2	16, 20, 24	
1080p 576p/i	YCbCr 4:4:4 RGB YCbCr 4:4:4	24, 30, 36	50/60 50
	YCbCr 4:2:2	16, 20, 24	
720p	RGB YCbCr 4:4:4	24, 30, 36	50/60
	YCbCr 4:2:2	16, 20, 24	
1080i	RGB YCbCr 4:4:4	24, 30, 36	50/60
	YCbCr 4:2:2	16, 20, 24	
	RGB	24, 30, 36	
	YCbCr 4:2:2	16, 20, 24	
4K x 2K	RGB YCbCr 4:4:4	24	24/25/30
	YCbCr 4:2:2	16, 20, 24	
	YCbCr 4:2:0	12	50/60

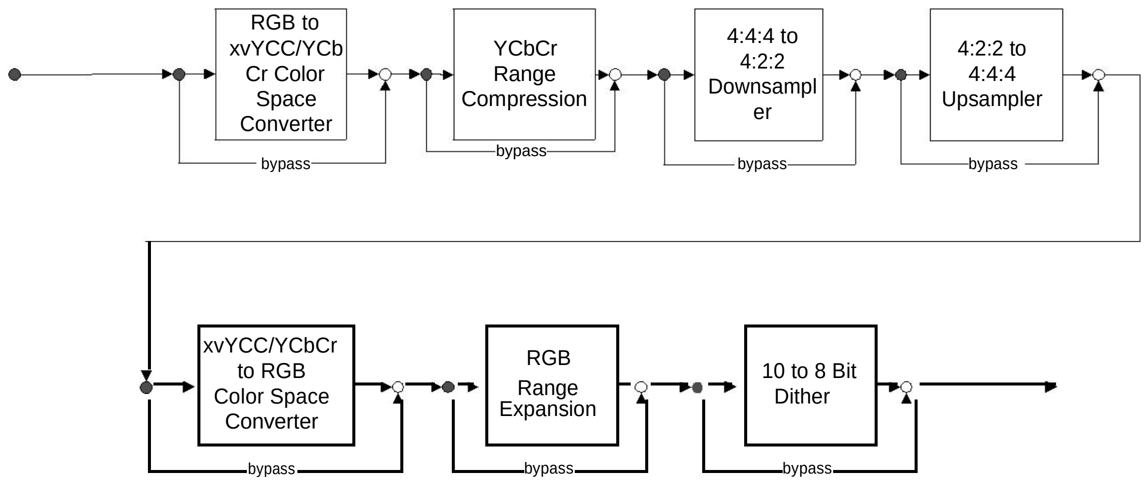
Notes:

1. the 4K x 2K YCbCr 4:2:0 mat, no video data conversion is supported.
2. deep color mats, no video data conversion is supported.

2.2. Video Data Conversion Logic Block

The SiI9678 HDMI transmitter supports Video Data Conversion Logic Block. Figure 2.2 shows the processing stages the video data. Each of the processing blocks can be bypassed by setting the appropriate register bits.

The 4K x 2K YCbCr 4:2:0 @ 50/60 Hz video mat and deep color video mats are not supported in the Video Data Conversion Logic Block. Theree, these mats will be bypassed by this block automatically.



2.2.1. Color Space Converters

Color Space Converters (CSCs) are provided to convert RGB data to the Standard-Definition (ITU.601) or High-Definition (ITU.709) YCbCr mats, and vice-versa. To support the latest extended-gamut xvYCC displays, the SiI9678 device

implements color space converter blocks to convert RGB data to the extended-gamut Standard-Definition (ITU.601) or High-Definition (ITU.709) xvYCC mats, and vice-versa. The CSC can be adjusted to perm standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

The SiI9678 transmitter adds supporttheextendedgamutxvYCC color space in the HDMI mode. This extended beca of the availability of LED and laser-based light sources the next generation displays. This mat also makes

See the RGB to YCbCr Color Space Converter and YCbCr to RGB Color Space Converter sections on page 25 more inmation.

2.2.1.1. xvYCC Support

mat has roughly 1.8 times more colors than the RGB color space. The of the xvYCC color space is made possible the

of the full range values (1 – 254) in an 8-bit space instead of 16 – 235 in the RGB mat.

2.2.2. YCbCr Range Compression

When enabled by itself, the Range Compression Block compresses 0 – 255 full-range data into 16 – 235 limited-range data each video channel, and compresses to 16 – 240 the Cb and Cr channels. The color range scaling is linear.

2.2.3. 4:4:4 to 4:2:2 Downsampler

Downsampling reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

2.2.4. 4:2:2 to 4:4:4 Upsampler

Chrominance upsampling and downsampling increase or decrease the number of chrominance samples in each line of video. Upsampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

2.2.5. RGB Range Expansion

The SiI9678 device can scale the input color from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16 – 235 limited-range data into 0 – 255 each video channel. When the range expansion and the xvYCbCr/YCbCr to RGB color space converter are both enabled, the input conversion range the Cb and Cr channels is 16 – 240.

2.2.6. 10 to 8 Bit Dither

The 10 to 8 Bit Dither block dithers ly-processed 10-bit data to 8-bit data output.

2.3. Receiver HDCP 1.4 Authentication Logic Block

The Receiver HDCP1.4 Authentication Logic Block handles the task of establishing a secure link receiving protected content from the source SoC. This process involves exchanging security inmation with the source SoC over the DDC.

2.4. HDCP 1.4 Decryption Engine Block

The HDCP1.4 Decryption Engine Block handles the task of decrypt data coming from the HDMI input interface. The appropriate decryption key is applied to the HDCP1.4 decryption engine block to descramble the video, audio, and

auxiliary packets.

2.5. Transmitter HDCP Authentication Logic Block

The Transmitter HDCP Authentication Logic Block handles the task of establishing a secure link transmitting protected content to downstream device. It also has two parts: one is HDCP 2.2 authentication, and the other is HDCP 1.4 authentication.

2.6. HDCP 1.4/2.2Encryption Engine Block

Unlike the HDCP 1.x authentication, the authentication process HDCP 2.2 involves authentication and key exchange

(AKE), pairing downstream device, random number generation, locality check, and session key exchange (SKE). At the end of authentication, a communication path is established between the HDCP2.2 Transmitter and HDCP2.2 Receiver, to which authorized device can access.

The SiI9678 transmitter has two HDCP encryption engines: one is HDCP 2.2 encryption engine, the other is HDCP 1.4 encryption engine.

The HDCP encryption engine contains the logic necessary to encrypt the incoming audio and video data and includes support HDCP authentication check. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes.

2.7. HDMI TMDS Transmitter Block

The HDMI TMDS Transmitter Block can drive out a fully compliant HDMI stream, based on the specific registers settings through the API interface.

an HDMI stream, the video, audio, and auxiliary data are transmitted through three TMDS data channels along with a TMDS differential clock.

2.8. One-Time Programmable Block

The SiI9678 transmitter comes preprogrammed with a set of production HDCP keys stored in an ROM. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. handles all purchasing, programming, and security the HDCP keys. The preprogrammed HDCP keys provide the highest level of security beca there is no way to read the keys once the devices are programmed. Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with bee receiving samples of the transmitter.

2.9. Serial Peripheral Interface Logic Block

The Serial Peripheral Interface (SPI) Logic Block provides an SPI Master interface. This SPI master interface is sampled once at reset to load the data from the external Flash/EEPROM when chip works in the stand-alone mode.
Usually, the SPI master logic is disabled in the normal working mode, except when the ISP block is enabled. Refer to the In-System-Program Block section below more details.

2.10.In-System-Program Block

The SiI9678 transmitter supports In-System-Program (ISP) firmware upgrade. The firmware code is stored in the external Flash/EEPROM device that connected to the SPI interface. The ISP Block provides a connection between the Local I^2C Slave Logic and the SPI Logic. With this ISP block, the external SoC can program the new code into the external Flash/EEPROM device directly through the local I^2C slave interface.

2.11.Microcontroller Unit

The SiI9678 transmitter has an MCU Microcontroller Unit (MCU) that provides a low-cost system

implementation. It is d to control the main data flow byregister configuration and interrupt handling, as well as
handle the initialization at reset, HDCP 1.4/2.2 authentication and encryption etc. This MCU will boot from the
external Flash/EEPROM through the SPI master interface.

2.12. Oscillator

The SiI9678 transmitter has an Oscillator (OSC) that provides the driving clock of the MCU
stand-alone mode. The frequency of this oscillator is 20MHz, which is calibrated in the factory. If oscillator is

2.13.Logic I2C Slave LogicBlock

The local I^2C slave bus provides a communication interface from the host to the SiI9678 device. The controller I^2C
chosen, external crystal will not be needed. However, the MCU can the external crystal as the clock source and

disable the oscillator as well.

interface on the SiI9678 transmitter (signals CSCL and CSDA) is a slave interface capable of running up to 400 kHz. See parametric limitation above 100 kHz in Table 3.9 on page 19. The host s this interface to configure the SiI9678 transmitter by reading from and writing to appropriate registers.

I^2C addresses of the device can be altered with the level of the CI2CA/GPIO4/GPIO5 signal, as described in the Device Address Configuration Using CI2CA/GPIO4/GPIO5 section on page 26.

2.14.Configuration, Status, and Interrupt Control Logic Block

The configuration block is d to configure and control the device operation, which can operate in either stand-alone mode (with MCU enabled) or in External MCU mode.

The Power-On Reset (POR) circuit is also contained in this block. POR provides an on-chip reset function to eliminate the need from an external POR circuit.

The level on INT pin is latched when the POR circuit transits from the asserted state to the de-asserted state. If the latched status is HIGH, the stand-alone mode will be selected. Otherwise, External MCU mode will be selected.

In the stand-alone mode, the SiI9678 chip requires an SPI flash/EEPROM firmware code storage and load the code to the MCU after the POR. All chip registers will be configured by the MCU. This mode supports ISP function firmware update.

In the External MCU mode, the SiI9678 chip requires an external I^2C master such as MCU/SoC chip registers configuration or external Flash/EEPROM device programming with In-System-Program (ISP) block.

Figure 2.3 and Figure 2.4 show the connection of the local I^2C port, SPI interface, and INT signal in stand-alone mode or in External MCU mode.

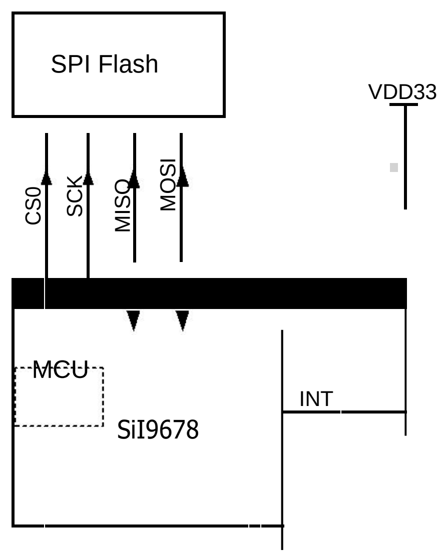


Figure 2.3. Stand-alone Mode

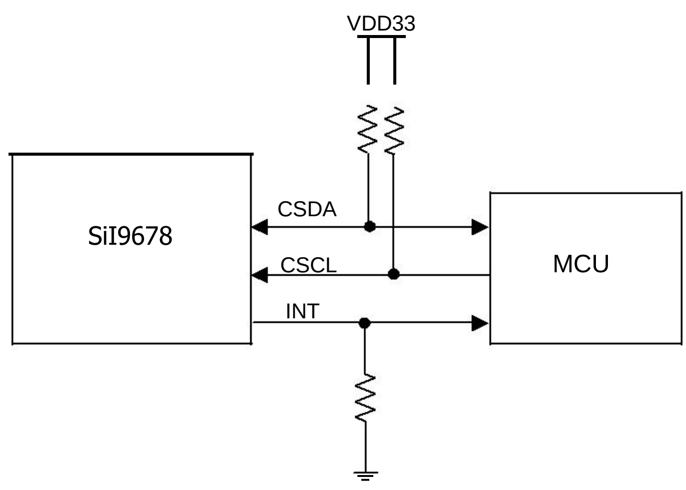


Figure 2.4. External MCU Mode

The INT signal interrupts the host processor when certain conditions arise inside the SiI9678 transmitter. The INT output is programmable to be either active HIGH or active LOW.

customers, an API adapter driver will be provided by hardware independent interface between the SiI9678 device and the customer application software. Refer to the SiI9678 API Reference (SiI-AR-1003) more details.

2.15.DDC Slave Block

The SiI9678 transmitter s an HDMI source as the input source. The DDC Slave Block is d the HDMI source to read the EDID from the SiI9678 transmitter.

2.16.DDC Master Block

The SiI9678 transmitter has a DDC Master the HDMI downstream device connection. The DDC master port is d direct connection to the HDMI cable. DDC read and write operations are executed by reading and writing registers in the transmitter. This feature simplifies the system design and helps to lower its cost.

2.17.On-Chip Regulation

The on-chip regulators provide a low-cost system implementation. The SiI9678 transmitter has two regulators: 3.3 V Regulator and 1.2 V Regulator. Both regulators are provided usage .
Each of the regulators has one output pin. The output pins are VDD33OUT and VDD12OUT. All these pins cannot be d as any external power supply, but require a separate 4.7 µF capacitor to ground each of the pin.

3. Electrical Specifications

3.1. Absolute Maximum Conditions

Table 3.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
XTAL_VDD33	XTAL Power Supply	–0.3	—	4.0	V	1, 2
VDD33	3.3 V Analog Power Supply	–0.3	—	4.0	V	1, 2
VDDIO33	Digital I/O Power Supply	–0.3	—	4.0	V	1, 2
AVDD33	Analog Driver Power Supply	–0.3	—	4.0	V	1, 2
VDD10	Digital Core Power Supply	–0.3	—	1.25	V	1, 2
AVDD10	Analog Receiver PHY Power Supply	–0.3	—	1.25	V	1, 2
AVDD10_PLL	Analog PLL Power	–0.3	—	1.25	V	1, 2
AVDD10_DP	Analog Data Path Power	–0.3	—	1.25	V	1, 2
AVDD10_OSC	Power Supply of Oscillator	–0.3	—	1.25	V	1, 2
FVDD10	Fractional PLL Power	–0.3	—	1.25	V	1, 2
RPWR5V	5 V Input from Power Pin of HDMI Connector	–0.3	—	5.7	V	1, 2
VDD5V_IN	Local Power 5 V Input	–0.3	—	5.7	V	1, 2
LPSBV5V	Low Power Standby 5 V Input	–0.3	—	5.7	V	1, 2
V_I	Input Voltage	–0.3	—	VDDIO33 + 0.3	V	1, 2
V_O	Output Voltage	–0.3	—	VDDIO33 + 0.3	V	1, 2
V_{I5V}	Input Voltage, 5 V Tolerant I/O	–0.3	—	5.5	V	1, 2, 4
V_{O5V}	Output Voltage, 5 V Tolerant I/O	–0.3	—	5.5	V	1, 2, 4
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. This is 5V tolerant pins, such as TX _HPD, RX HPD, DSCL, DSDA, INT, TDSCL, TDSDA, CSCL, CSDA, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, and GPIO5.

3.2. Normal Operating Conditions

Table 3.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
XTAL_VDD33	XTAL Power Supply	3.13	3.3	3.47	V	—
VDD33	3.3 V termination Power Supply	3.13	3.3	3.47	V	1
VDDIO33	Digital I/O Power Supply	3.13	3.3	3.47	V	—
AVDD33	Analog Driver Power Supply	3.13	3.3	3.47	V	—
VDD10	Digital Core Power Supply	0.95	1.0	1.05	V	—
AVDD10	Analog Receiver PHY Power Supply	0.95	1.0	1.05	V	—
AVDD10_PLL	Analog PLL Power	0.95	1.0	1.05	V	—
AVDD10_DP	Analog Data Path Power	0.95	1.0	1.05	V	—
AVDD10_OSC	Power Supply of Oscillator	0.95	1.0	1.05	V	—
FVDD10	Fractional PLL Power	0.95	1.0	1.05	V	—
RPWR5V	5 V Input from Power Pin of HDMI Connector	4.3	5.0	5.25	V	—
VDD5V_IN	Local Power 5 V Input	4.3	5.0	5.25	V	—
LPSBV5V	Low Power Standby 5 V Input	4.75	5.0	5.25	V	—
V_{DDN}	Allowable Supply Voltage Noise	—	—	100	mV_{P-P}	2
T_A	Ambient Temperature (with power applied)	–30	25	85	°C	—
Θ_{ja}	Ambient Thermal resistance (Theta JA)	—	—	28.0	°C/W	3
Θ_{jc}	Ambient Thermal resistance (Theta JC)	—	—	14.4	°C/W	3

Notes:

1. The HDMI Specification requires 3.3 V ±5% termination voltage (VDD33).
2. The supply voltage noise is measured in testing point VDDTP as shown in Figure 3.1. The ferrite bead provides filtering of power supply noise.
3. Values Θ_{ja} and Θ_{jc} are provided fpr 4-layer PCB, Airflow at 0 m/s.

See the Power Supplies Decoupling section on page 28 the recommended decoupling and power supply regulation.

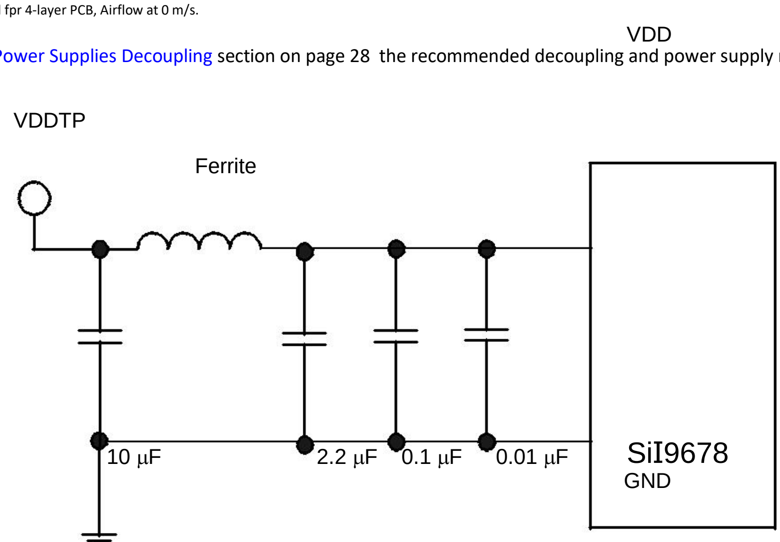


Figure 3.1. Test Point VDDTP VDD Noise Tolerance Specification

3.2.1. Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Table 3.3. DC Digital I/O Specifications

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH Level Input Voltage	LVTTL	—	2.0	—	—	V	2
V_{IL}	LOW Level Input Voltage	LVTTL	—	—	—	0.8	V	2
V_{TH+DDC}	LOW to HIGH Threshold, DDC bus	Schmitt	—	3.5	—	—	V	5, 8
V_{TH-DDC}	HIGH to LOW Threshold DDC bus	Schmitt	—	—	—	1.5	V	5, 8
$V_{TH+RESETN}$	LOW to HIGH threshold, RESETN pin	Schmitt	—	2.0	—	—	V	—
$V_{TH-RESETN}$	HIGH to LOW threshold, RESETN pin	Schmitt	—	—	—	0.8	V	—
V_{TH+I2C}	LOW to HIGH Threshold, I^2C Bus	Schmitt	—		2.0—	—	V	—
V_{TH-I2C}	HIGH to LOW Threshold, I^2C Bus	Schmitt	—	—	—	0.8	V	—
V_{OH}	HIGH Level Output Voltage	LVTTL Open Drain	I_{OH} = 3 mA	2.4	—	—	V	—
V_{OL}	LOW Level Output Voltage	LVTTL Open Drain	I_{OL} = 3 mA	—	—	0.4	V	—
I_{IL}/I_{IH}	Input Leakage Current	—	—	−10	—	10	µA	—
TX_HPD I_{IL}/I_{IH}	Input Leakage Current	—	—	-30	—	30	µA	—
I_{OD}	General Digital Output Drive	Output	V_{OH} = 2.4 V	7.5	—	—	mA	1, 6, 7
			V_{OL} = 0.4 V		—	—	mA	1, 6, 7

Notes:

1. These limits are guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading C_L = 10 pF.
3. Refer to the Pin Descriptions section on page 21 pin type designations all package pins.
4. Differential input voltage is a single-ended measurement, according to the DVI Specification.
5. these Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, are respectively guaranteed by design.
6. Minimum output drive specified at ambient = 70 °C and VDD33 = 3.0 V. Typical output drive specified at ambient =25 °C and VDD33 = 3.3 V. Maximum output drive specified at ambient = −20 °C and VDD33 = 3.6 V.
7. I_{OD} Output applies to all pins defined as LVTTL and LVTTL/Schmitt trigger.
8. I_{ODDDC} Output applies to all pins defined as Schmitt trigger.

Table 3.4. TMDS Input DC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDF}	Differential Mode Input Swing Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Swing Voltage	—	V_{TERM} – 400	—	V_{TERM} – 37.5	mV

Table 3.5. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VSWING	Single-ended Output Swing Voltage	RLOAD = 50 Ω	400	—	600	mV
VH	Single-ended HIGH-level Output Voltage	—	AVDD33 – 200	—	AVDD33 + 10	mV
VL	Single-ended LOW-level Output Voltage	—	AVDD33 – 700	—	AVDD33 – 400	mV

3.2.2. DC Power Consumption

Table 3.6. DC Power Consumption

Symbol	Parameter	Output Frequency	Typical			Maximum			Units	Notes
			5 V	3.3 V	1.0 V	5.5 V	3.63 V	1.1 V		
I_{DDSB}	Standby Current	—	7.2	8.9	133	8.4	9.1	195	mA	1
I_{DDFP}	Full Operation Current	720x480p60	7.3	53.9	165	8.4	54.5	259	mA	2
		1920x1080p60	7.3	53.5	200	8.4	54.1	312	mA	2
		4Kx2Kp30	7.3	52.9	272	8.4	53.5	414	mA	2

Notes:

1. All power nets are supplied and no input and output are connected.
2. Test results will differ pending on TMDS driving current settings of the HDMI source.

3.3. AC Specification

T_{IJIT} Differential Input Clock Jitter Tolerance 165 MHz—

3.3.1. TMDS AC Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 3.7. TMDS Input Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{INTRA-PAIR\_SKEW}$	Input Intra-pair Skew	—	—	—	0.4	T_{BIT}
$T_{INTER-PAIR\_SKEW}$	Input Inter-pair Skew	—	—	—	$0.2T_{PIXEL} + 1.78$	ns
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns
				—	0.3	T_{BIT}

Table 3.8. TMDS Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TXDPS}	Intra-Pair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRT}	Data/Clock Rise Time	—	75	—	—	ps
T_{TXFT}	Data/Clock Fall Time	—	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DUTY}	Differential Output Clock Duty Cycle	—	40	—	60	T_{TXC}
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}

3.3.2. Control Signal Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 3.9. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{RESET_VDD}	Time required RESETN high bee VDD	50% RESETN to 90% VDD	1	—	—	µs	Figure 4.1	—
T_{RESET}	RESETN signal LOW time required reset	—	2	—	—	ms	Figure 4.2	1, 5
T_{I2CDVD}	SDA data valid delay from SCL falling edge on READ command	C_L = 400 pF	—	—	700	ns	Figure 4.3	2, 6
T_{HDDAT}	I^2C data hold time	0 – 400 kHz	2.0	—	—	ns	—	3, 6
T_{INT}	Response time INT output signal from change in input condition (HPD, Receiver Sense, VSYNC Change etc.).	RESETN = HIGH	—	—	100	µs	Figure 4.4	—
F_{TDSCL}	Frequency of DDC master TDSCL signal	—	40	70	100	kHz	—	4
F_{CSCL}	levels, I^2C speeds up to 400 kHz are supported. Frequency of local I^2C CSCL signal	—	40	—	400	kHz	—	—

Notes:

1. Reset on RESETN signal can be LOW as the supply becomes stable, as shown in Figure 4.1, or pulled LOW at least T_{RESET} as shown in Figure 4.2.
2. All standard-mode (100 kHz) I^2C timing requirements are guaranteed by design. These timings apply to the slave I^2C port (pins CSDA and CSCL) and to the master I^2C port (pins DSDA and DSCL).
3. This minimum hold time is required by CSCL and CSDA signals as an I^2C slave. The device does not include the 300 ns delay required by the I^2C Specification.
4. The DDC master block provides a TDSCL signal the transmitter DDC bus. The HDMI Specification limits this to I^2C Standard Mode or 100 kHz. of the Master DDC block does not require an active IDCK.
5. Not a Schmitt trigger.
6. Operation of I^2C pins above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL} . See Table 3.3 on page 17. these

3.3.3. ESD Specifications

Table 3.10. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
Latch up	ESD Latch up	± 200	—	—	mA	1, 2
HBM	Human Body Model	2000	—	—	V	3
CDM	Charged Device Model	500	—	—	V	5

2. Measured according to JESD78B standard.

Notes:

1. Test is permed at 70 °C.

3. Measured according to JESD22-A114 standard.
4. Measured according to JESD22-A115 standard.
5. Measured according to JESD22-C101 standard.

4. Timing Diagrams

4.1. RESETTN Timing Diagrams

Power sequencing is not required the SiI9678 transmitter. However, to ensure a proper reset the rules mentioned under the diagrams in Figure 4.1 and Figure 4.2 must be followed.

VDD10 must be stable between its limits Normal Operating Conditions T_{RESET_VDD} bee RESETN goes high, as shown in Figure 4.1. Bee accessing registers, RESETN must be pulled low T_{RESET}. This can be done by holding RESETN low until T_{RESET_VDD} after stable power, as described above, or by pulling RESETN low from a high state at least T_{RESET}, as shown in Figure 4.2.

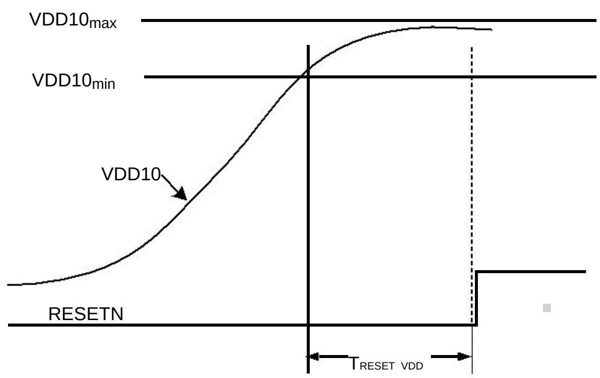


Figure 4.1. Conditions   of RESETN

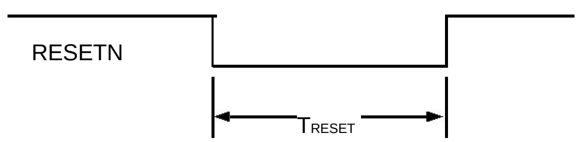


Figure 4.2. RESETN Minimum Timings

4.2. Output Timing Diagrams

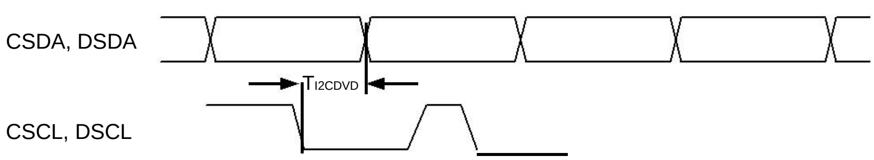


Figure 4.3. I^{2}C Data Valid Delay (Driving Read Cycle Data)

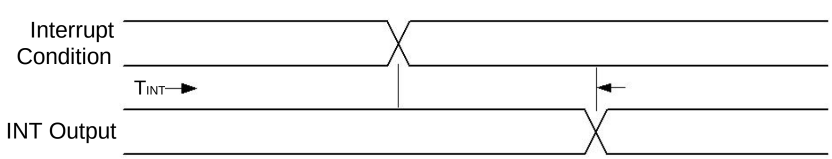


Figure 4.4. INT Output Signal Response to Interrupt Condition

5. Pin Descriptions

The following tables provide the pin descriptions the SiI9678 transmitter.

5.1. HDMI Input

Table 5.1. HDMI Input Pins

Pin Name	Pin	Type	Dir	Description
RXCN	7	TMDS	Input	HDMI Differential Clock Input.
RXCP	8	TMDS	Input	
RX0N	11	TMDS	Input	HDMI Differential Channel 0 Data Input.
RX0P	12	TMDS	Input	
RX1N	13	TMDS	Input	HDMI Differential Channel 1 Data Input.
RX1P	14	TMDS	Input	
RX2N	15	TMDS	Input	HDMI Differential Channel2 Data Input.
RX2P	16	TMDS	Input	
RX_HPD	4	5 V tolerant	Output	HPD (Hot-plug Detect) Output of HDMI RX side.
DSCL	75	Schmitt 5 V tolerant Open-drain	Input	DDC Clock and Data of HDMI RX side. These signals are true open-drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSDA	76	Schmitt 5 V tolerant Open-drain	Input/ Output	

5.2. HDMI Output

Table 5.2. HDMI Output Pins

Pin Name	Pin	Type	Dir	Description
TXCN	40	TMDS	Input	HDMI Differential Clock Output.
TXCP	41	TMDSInput		
TX0N	42	TMDS	Input	HDMI Differential Channel 0 Output.
TX0P	43	TMDS	Input	
TX1N	44	TMDS	Input	HDMI Differential Channel 1 Output.
TX1P	45	TMDS	Input	
TX2N	46	TMDS	Input	HDMI Differential Channel 2 Output.
TX2P	47	TMDS	Input	
[redacted]				
TX_HPD	38	5 V tolerant	Input	Hot-plug Detect Input. An external 10 kΩ pull-down resistor is required on this pin.
TDSCL	66	Schmitt 5 V tolerant Open-drain	Input/ Output	DDC Clock and Data of TX side (I^2C Master). These pins implement true open-drain circuits; external pull-up (1.8 kΩ ±10% typical) resistors to DDC 5 V are required. These are 5 V tolerant pins.
TDSDA	67	Schmitt 5 V tolerant Open-drain	Input/ Output	

5.3. External XTAL Pins

Table 5.3. External XTAL Pins

Pin Name	Pin	Type	Dir	Description
XTAL_IN	49	LVTTL	Input	Clock Input external crystal. This pin can be NC when OSC is d.
XTAL_OUT	50	LVTTL	Output	Clock Output external crystal. This pin can be NC when OSC is d.

5.4. Control and Configuration Pins

Table 5.4. Control and Configuration Pins

Pin Name	Pin	Type	Dir	Description
RESETN	34	LVTTL Schmitt	Input	External Reset pin (Active LOW) . This pin should not be left floating.An external 4.7 kΩ pull-up resistor to 3.3 V is required.
CSCL	68	LVTTL Schmitt Open-drain 5 V tolerant	Input	Local I²C Bus Clock. This bus is d accessing the device registers. This pin is true open drain, so it does not pull to ground if no power is applied. normal operation, an external 4.7 kΩ pull-up resistor to 3.3 V is required.
CSDA	69	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local I²C Bus Data. This bus is d accessing the device registers. This pin is true open drain, so it does not pull to ground if no power is applied. normal operation, an external 4.7 kΩ pull-up resistor to 3.3 V is required.
TMODE	25	LVTTL Schmitt 5 V tolerant	Input	Test Mode Enable. Pull down normal operation.
INT	20	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	MCU Enable Input during POR or Interrupt Output in Normal Operation. This is an open-drain output and requires an external pull-up resistor. During the power-on reset (POR), this pin is d as an input to latch the MCU enabled or not. The level on this pin is latched when the POR transitionsfrom the asserted state to the deasserted state. After completion of POR, this pin is d as interrupt output, which defaults active LOW.
GPIO0_CI2CA	21	LVTTL 5 V tolerant Schmitt Open-drain	Input/ Output	General Purpose I/O 0 or CI2CA. This pin defaults to an input and is sampled once at reset to select the local I²C target address ranges.
GPIO1	22	LVTTL 5 V tolerant Schmitt Open-drain	Input/ Output	General Purpose I/O 1. This pin defaults to an output.
GPIO2	23	LVTTL 5 V tolerant Schmitt Open-drain	Input/ Output	General Purpose I/O 2. This pin defaults to an input.
GPIO3	30	LVTTL 5 V tolerant Schmitt Open-drain	Input/ Output	General Purpose I/O 3. This pin defaults to an input.
GPIO4	31	LVTTL 5 V tolerant Schmitt Open-drain	Input/ Output	General Purpose I/O 4. This pin defaults to an input.

Table 5.4. Control and Configuration Pins (Continued)

Pin Name	Pin	Type	Dir	Description
GPIO5	32	LVTTL 5 V tolerant Schmitt Open-drain	Input/ Output	General Purpose I/O 5. This pin defaults to an input.
SPI_CLK	60	LVTTL	Input/ Output	SPI Master Interface stand-alone mode. This interface is sampled once at reset to load the data from the external Flash/EEPROM. This interface is disabled in the normal working mode, except when the ISP block is enabled.
SPI_CS0	61	LVTTL	Output	
SPI_MOSI	63	LVTTL	Input/ Output	
SPI_MISO	64	LVTTL	Input/ Output	

5.5. Power and Ground Pins

Table 5.5. Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
XTAL_VDD33	48	Power	XTAL Power.	3.3 V
XTAL_GND	51	Ground	XTAL Ground.	Ground
AVDD33	37	Power	Analog Driver Power Supply	3.3 V
VDD33	10,57	Power	Receiver Termination 3.3 V Power.	3.3 V
AVDD10_PLL	36	Power	Analog PLL Power.	1.0 V
VDDIO33	19, 33, 65	Power	Digital I/O Power.	3.3 V
VDD10	24, 35, 58, 59, 70	Power	Digital Core Power.	1.0 V
GND	5,55	Ground	Ground pin.	Ground
AVDD10	6,9,17	Power	Analog Receiver PHY Power.	1.0 V
AVDD10_DP	39	Power	Analog Data Path Power.	1.0 V
AVDD10_OSC	52	Power	Analog power of oscillator	1.0 V
FVDD10	18	Power	Fractional PLL Power.	1.0 V
VDD5V_IN	2	Power	Local Power 5 V Input. If there is no RPWR5V input, an active 5 V power input of this pin is required.	5 V
RPWR5V	3	Power	5 V Port Detection Input the HDMI Input Port. Connect to 5 V signal from HDMI input connector. This pin requires a 10 Ω series resistor, a 5.1 KΩ pull-down resistor, and at least a 1 µF capacitor to ground.	5 V
LPSBV5V	74	Power	Low Power Standby 5 V Input.	5 V
VDD33OUT	1	Power	3.3 V Regulator Output. This pin requires a 4.7 µF capacitor to ground. Must not be d as any external power supply.	—
VDD12OUT	56	Power	1.2 V Regulator Output. This pin requires a 4.7 µF capacitor to ground. Must not be d as any external power supply.	—
GND	ePad	Ground	Ground. All ground connections to the device are through the ePad, theree it must be soldered to the board and the pad must have a low resistance connection to the board ground plane.	Ground

5.6. Reserved and Not Connected Pins

Table 5.6. Reserved and Not Connected Pins

Name	Pin	Type	Description	Supply
RSVDL	73	RSVD	These pins must be connected to LOW.	—
NC	26, 27, 28, 29, 53, 54, 62, 71, 72	RSVD	No connection.	—

6. Feature Inmation

6.1. RGB to YCbCr Color Space Converter

The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr mats. Table 6.1 shows the conversion mulas that are d. The HDMI AVI packet defines the color space of the incoming video.

Table 6.1. RGB to YCbCr Conversion mulas

Video mat	Conversion	mulas CE Mode 16-235 RGB
VGA	ITU-R BT.601	Y = 0.299R′ + 0.587G′ + 0.114B′ Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
WVGA	ITU-R BT.601	
SVGA	ITU-R BT.601	
480p/i	ITU-R BT.601	
576p/i	ITU-R BT.601	
XGA	ITU-R BT.709	Y = 0.213R′ + 0.715G′ + 0.072B′ Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
SXGA	ITU-R BT.709	
UXGA	ITU-R BT.709	
WUXGA	ITU-R BT.709	
720p	ITU-R BT.709	
1080i	ITU-R BT.709	
1080p	ITU-R BT.709	
4K x 2K	ITU-R BT.709	

Table 6.2. YCbCr-to-RGB Conversion mulas

Note the difference between RGB range CE modes and PC modes.

6.2. YCbCr to RGB Color Space Converter

The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB- inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. See Table 6.2 the detailed mulas.

R′= Y + 1.540(Cr – 128)

	709	G′ = Y – 0.459(Cr – 128) – 0.183(Cb – 128)
mat Change	**Conversion**	**YCbCr Input Color Range**
RGB 16-235 Output	601*	R′ = Y + 1.371(Cr – 128) G′ = Y – 0.698(Cr – 128) – 0.336(Cb – 128) B′ = Y + 1.816(Cb – 128)
YCbCr 16-235 Input to RGB 0-255 Output	601	R′ = 1.164((Y-16) + 1.371(Cr – 128)) G′ = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B′ = 1.164((Y-16) + 1.732(Cb – 128))
	709	R′ = 1.164((Y-16) + 1.540(Cr – 128)) G′ = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B′ = 1.164((Y-16) + 1.816(Cb – 128))

***Note:** No clipping can be done.

6.3. 3D Video mats

The SiI9678 transmitter supports the 3D video modes described in the HDMI 1.4a Specification. All modes support RGB 4:4:4, YCbCr 4:2:2, and YCbCr 4:4:4 color mats and 8-bit color depth. Table 6.3 shows the maximum possible resolution with a given frame rate. example, Side-by-Side mode is defined 1080p @ 60 Hz frame, which implies that 720p @ 60 Hz and 480p @ 60 Hz are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz and its associated pixel frequency is supported.

Table 6.3. Supported HDMI 3D Input Video mats

HDMI 3D mat	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	
Side-by-Side	Full	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	148.5
	Half	4K*2K	24/30	300
		1080p	50/60	148.5
Top-and-Bottom	—	4K*2K	24/30	300
		1080p	50/60	148.5
		1080p	24/30	74.25
		720p/1080i	50/60	
Line Alternative	—	1080p	50/60	300
		1080p	24/30	
Field Alternative	—	1080i	50/60	
L + Depth	—	1080p	50/60	300
		1080p	24/30	148.5
		720p/1080i	50/60	

6.4. Device Address Configuration Using CI2CA/GPIO4/GPIO5

All functions of the SiI9678 transmitter are controlled and observed with I^{2}C registers. The I^{2}C address of the device depends on the working mode: External MCU mode or Stand-alone mode. The GPIO0_CI2CA/GPIO4/GPIO5 pins default to an input signal and are sampled once at reset to select the local I^{2}C target address ranges.

External MCU mode, CI2CA signal is d the local I^{2}C target address selection which is fixed to 0x60/0x62. Refer to Table 21. Beside the I^{2}C address of Page0, other visible slave addresses on the I^{2}C bus include: 0x10, 0x20, 0x30, 0x40, 0x50, 0x56, 0x68, 0x72, 0x7A, 0x80, 0x8A, 0x92, 0xC0, 0xD0, 0xE0 and 0xF0, system application should avoid these addresses.

Table 6.4. Control of I^{2}C Address with CI2CA Signal

Local I^{2}C address of Page 0	CI2CA
0x60	Low
0x62	High

Stand-alone mode, GPIO4 and/or GPIO5 signals are d the local I^2C target address selection which is defined by the firmware of MCU. Refer to Table 6.5.

Table 6.5. Control of I^2C Address with GPIO4/GPIO5 Signal

Local I^2C address of Page 0	GPIO4	GPIO5	Notes
Value1	Low	Low	1, 2
Value2	Low	High	1, 2
Value3	High	Low	1, 2
Value4	High	High	1, 2

Notes:

1. The I^2C address value is defined by firmware of the MCU.
2. Value1, 2, 3, and 4 are configurable based on system design requirement.

7. Design Recommendations

The tolerance of all resistors shown in this section is ± 5% unless otherwise noted.

7.1. Power Supplies Decoupling

Designers should include adequate decoupling capacitors and a ferrite each power supply, and an additional capacitor at each power pin in the layout. These are shown schematically in Figure 7.1. Place these components as close as possible to the SiI9678 device pins, and avoid routing through visa if possible, as shown in Figure 7.2, which represents a typical power connection on the SiI9678 device. Connections in one group (such as VDD) can share C2, the ferrite, and C3, with each pin having a separate C1 placed as closely to the pin as possible. Suggested values C1, C2, and C3 are 0.01 µF, 0.1 µF, and 10 µF, respectively. The recommended impedance of ferrite L1 is 10 Ω or more in the frequency range of 1 – 2 MHz all power supplies.

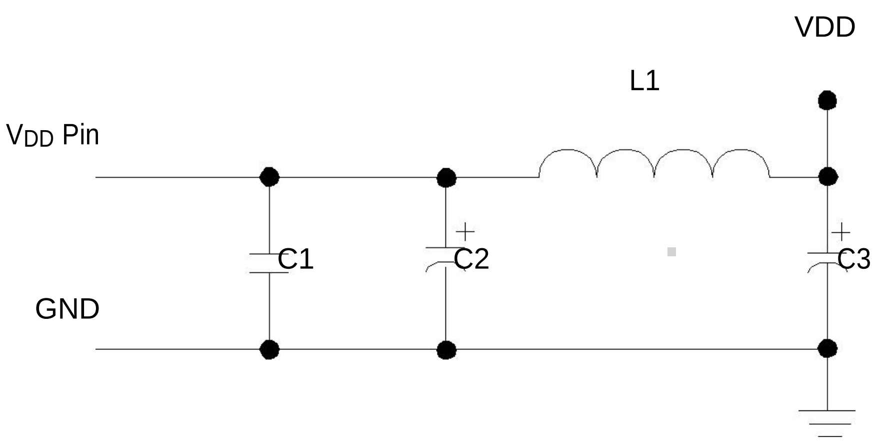


Figure 7.1. Decoupling and Bypass Schematic

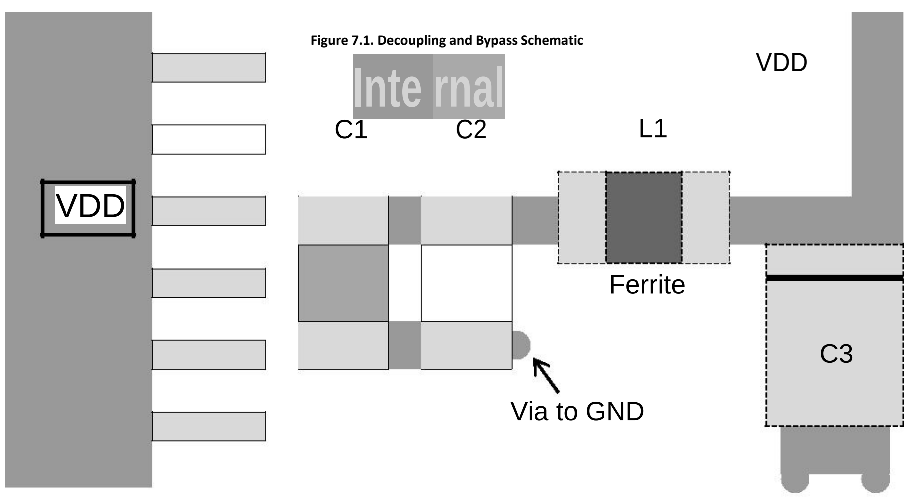


Figure 7.2. Decoupling and Bypass Capacitor Placement

7.2. High-speed TMDS Signals

7.2.1. Source Termination

Source termination suppresses signal reflection and overshoot, and at the same time allows the SiI9678 transmitter to provide strong drive to support longer cables. TheSiI9678 transmitter supports source termination, which is disabled by default and can be enabled by programming. strongly recommends the of source termination applications running over 100 MHz.

7.2.2. Transmitter Layout Guidelines

Place the SiI9678 transmitter chip as closely as possible to the output connector that carries the TMDS signals, and place the ESD diodes as closely as possible to the HDMI connector. Route the differential signal lines together and as directly as possible from SiI9678 transmitter to connector. TMDS devices are tolerant of skews between
through visa unless absolutely necessary when using the HDMI Type-D micro connector.The distance separating the two traces of the differential pair should be designed 100 Ω differential impedance.
differential pairs, so spiral skew compensation path length differences is not required. Avoid passing the TMDS lines

7.2.3. ESD Protection

The SiI9678 transmitter chip is designed to withstand electrostatic discharge during manufacturing handling. In applications where higher protection levels are required in the finished product, ESD-limiting components should be placed on all the device pins connecting to an external interface. Special care should be taken on the TMDS signals to low-capacitance ESD devices to minimize signal degradation. In no case should the capacitance value exceed 1 pF.

7.3. EMI Considerations

as possible, with all ground signals of the chip using a common ground.

HDMI is inherently low in EMI, as long as the routing recommendations noted in the Transmitter Layout Guidelines section are followed. Common mode choke is required by TMDS signals of transmitter side permance improvement to pass the HDMI CTS, we recommend using the component: DLW21SN670HQ2L.
Electromagnetic interference is a function of board layout, shielding, receiver component operating voltage, frequency

of operation, and additional factors. To control emissions, it is important not to place any passive components on the
differential signal lines, except the essential ESD protection describedearlier. The differential signaling d in

The PCB ground plane should extend unbroken under as much of the SiI9678 transmitter chip and associated circuitry

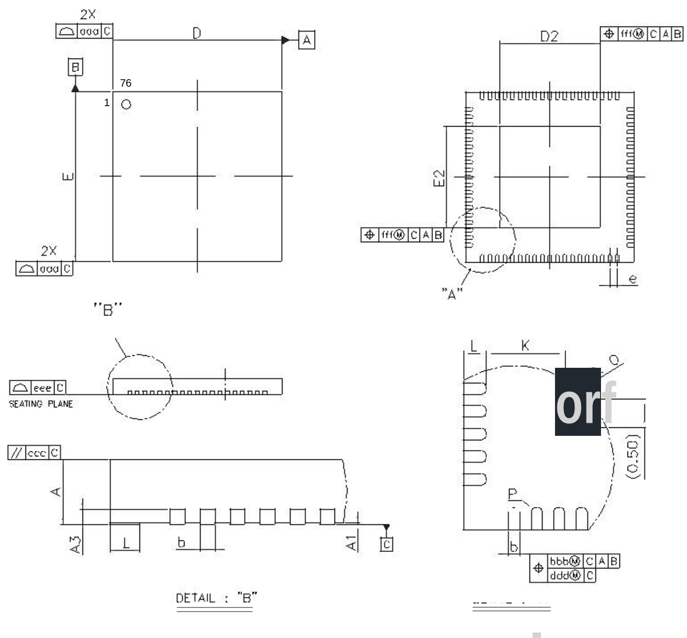
8. Packaging

8.1. ePad Requirements

The SiI9678 transmitter chip is packaged in a 76-pin, 9 mm × 9 mm QFN package with an exposed Pad (ePad) that is d electrical ground of the device and improving thermal transfer characteristics. The ePad dimensions are 6.3 mm × 6.3 mm shown on the following page. Soldering the ePad to the ground plane of the PCB is required to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. As a general guideline, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical short. Figure 8.1 on page 31 shows the package dimensions of the SiI9678 transmitter.

8.2. Package Dimensions

These drawings are not to scale.



JEDEC Package Code MO-220

Symbol	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
e	Lead pitch		0.40 BSC	
A1	Stand-off	0.00	0.02	0.05
A3	Base thickness		0.20 REF	
D / E	Body size	8.90	9.00	9.10
D2 / E2	ePad size	6.15	6.30	6.45
b	Plated lead width	0.15	0.20	0.25
ccc	—		0.10	
L	Lead foot length	0.30	0.40	0.50
ddd	—		0.05	
R	Lead tip radius	0.075	—	—
K	Lead to ePad clearance	0.20	—	—
aaa	—		0.10	
bbb	—		0.07	
eee	—		0.08	
fff	—		0.10	

All dimensions are in millimeters.

Figure 8.1. 76-pin QFN Package Diagram

8.3. Marking Specification

Figure 8.2 shows the marking of the SiI9678 package. Marking drawings are not to scale.

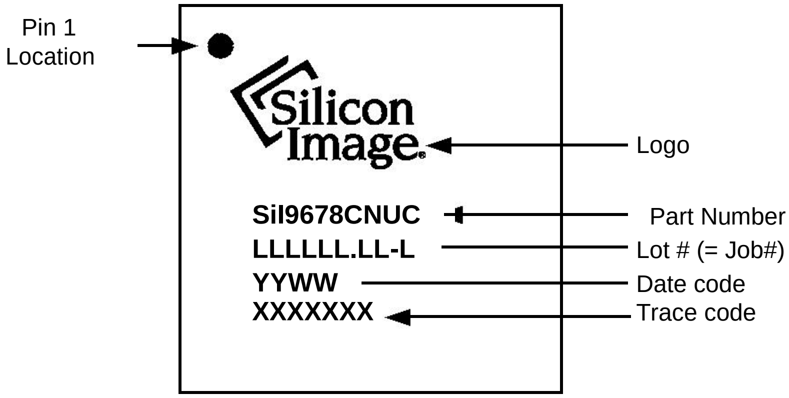


Figure 8.2. Marking Diagram

8.4. Ordering Inmation

Production Part Numbers:

Device	Part Number
SiI9678 HDMI Transmitter with HDCP2.2 Support	SiI9678 CNUC

The universal package can be d in both lead-free and ordinary process lines.

References

Standards Documents

This is a list of the standards abbreviations appearing in this document.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface,* Revision 1.4a, HDMI Consortium; March 2010
HCTS	*HDMI Compliance Test Specification,* Revision 1.4a, HDMI Consortium; March 2010
HDCP	*High-bandwidth Digital Content Protection,* Revision 1.3, Digital Content Protection, LLC; December 2006 *High-bandwidth Digital Content Protection,* Revision 2.2, Digital Content Protection, LLC; December 2011
MHL	*MHL (Mobile High-definition Link) Specification,* Version 3, MHL, LLC, Month 2013
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; Feb. 2000
E-EDID IG	*VESA EDID Implementation Guide*, Version 1.0, VESA; June 2001
CEA-861-E	*A DTV Profile Uncompressed High Speed Digital Interfaces,* EIA/CEA;March 2008
EDDC	*Enhanced Display Data Channel Standard,* Version 1.1, VESA; March 2004
I^2C	*The I^2C Bus Specification,* Version 2.1, Philips Semiconductors, January 2000

inmation on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL	e-mail	phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—
MHL	http://www.mhlconsortium.org	Customerservice@mhlconsortium.org	408-962-4269
I^2C	http://www.nxp.com	—	—

[redacted] Documents

This is a list of the related documents that are available from your sales representative.

Document	Title
SiI-UG-1127	*CP9678 HDMI Transmitter Starter Kit*
SiI-AR-1003	*SiI9678 and SiI9679 Adapter Driver*

Revision History

Revision B, April 2014

Updated Table 6.3. Supported HDMI 3D Input Video mats.

Revision A, March 2014

First production release.

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