


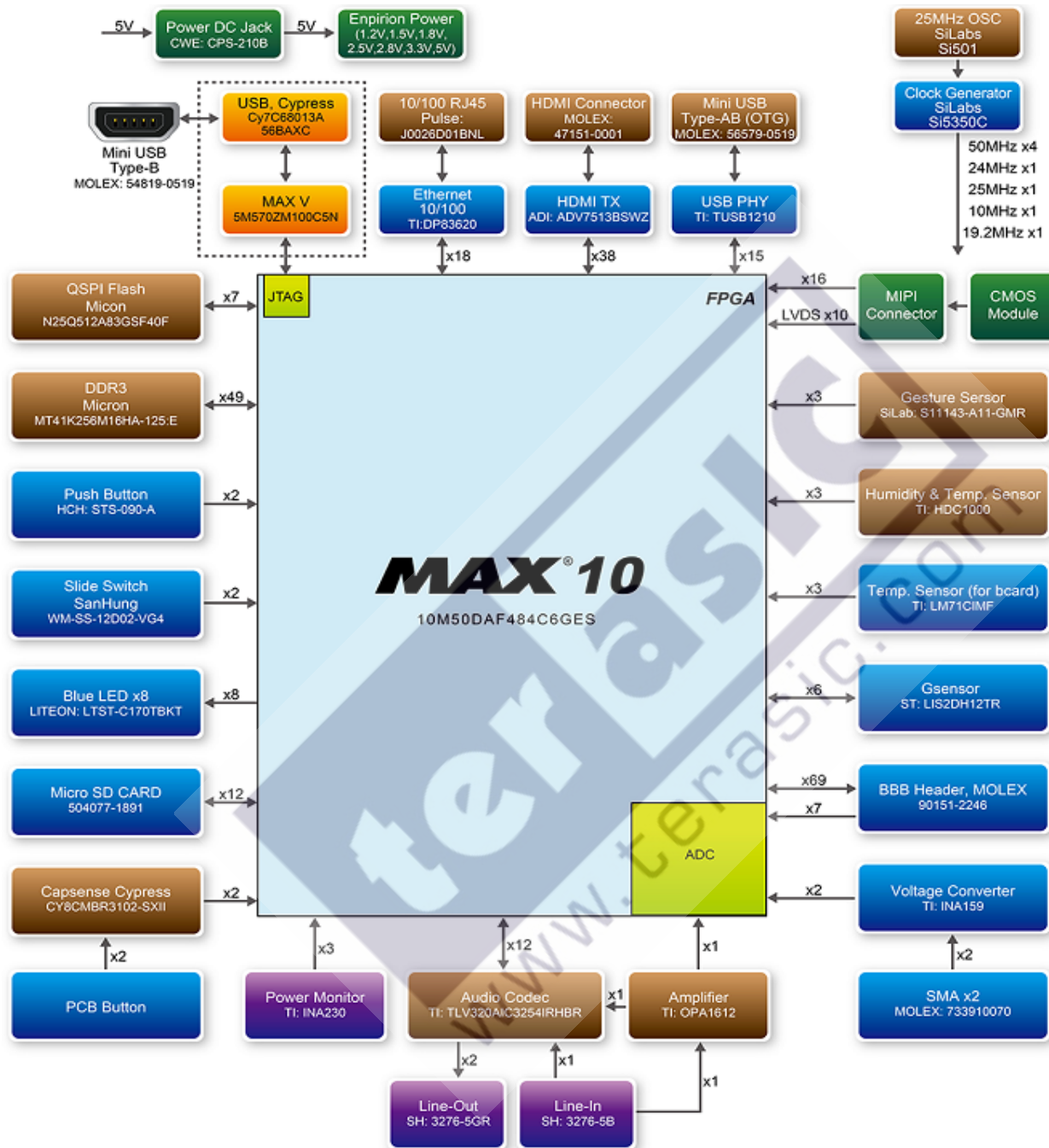
# DECA

Section	Title	Page
<b>01.0</b>	<b>Design Introduction</b>	
1.01	Cover Page	1
1.02	Block Diagram	2
<b>02.0</b>	<b>MAX 10 10M50DAF484</b>	
02.01	MAX 10 BANK1 & BANK2	3
02.02	MAX 10 BANK3 & BANK4	4
02.03	MAX 10 BANK5 & BANK6	5
02.04	MAX 10 BANK7 & BANK8	6
02.05	MAX 10 Clocks & Configuration	7
02.06	MAX10 Power & GND	8
02.07	MAX10 Decoupling	9
<b>03.0</b>	<b>Clock</b>	
03.01	Clock	10
<b>04.0</b>	<b>JTAG</b>	
04.01	USB Blaster II	11
<b>05.0</b>	<b>Expansion Port</b>	
05.01	Expansion Headers - BBB Headers	12
<b>06.0</b>	<b>Memory</b>	
06.01	DDR3 SDRAM & QSPI Flash	13
06.02	SD Card	14

09.02

Section	Title	Page
<b>07.0</b>	<b>Video &amp; Audio</b>	
07.01	MIPI Interface	15
07.02	HDMI TX	16
07.03	Audio CODEC	17
<b>08.0</b>	<b>Ethernet</b>	
08.01	Ethernet	18
<b>09.0</b>	<b>USB PHY</b>	
09.01	USB PHY	19
<b>10.0</b>	<b>Analog Interface</b>	
10.01	SMA Connectors & Differential Amplifier	20
<b>11.0</b>	<b>Sensors</b>	
11.01	Accelerometer	21
11.02	Gesture, Humidity, Temperature Sensors	22
<b>12.0</b>	<b>User Interface</b>	
12.01	LED & BUTTON & SWITCH	23
<b>13.0</b>	<b>System Power</b>	
13.01	1.2V & 1.5V & 1.8V & 5V	24
13.02	2.5V & 2.8V & 3.3V	25

 Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	Cover Page	C
Date:	Wednesday, March 11, 2015	Sheet 1 of 25

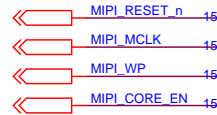


CAD Notes:  
 1. Put all the 1pF caps close to each MAX10 analog pin.  
 2. Route the analog input signal adjacent to the REFVDD.

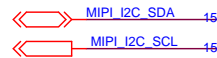
### MIPI Interface



### MIPI Control Interface



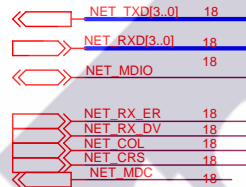
### MIPI I2C Interface



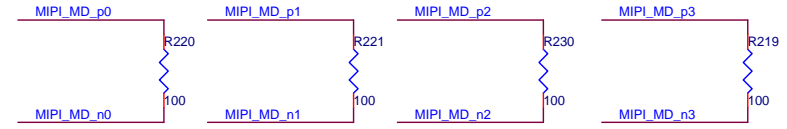
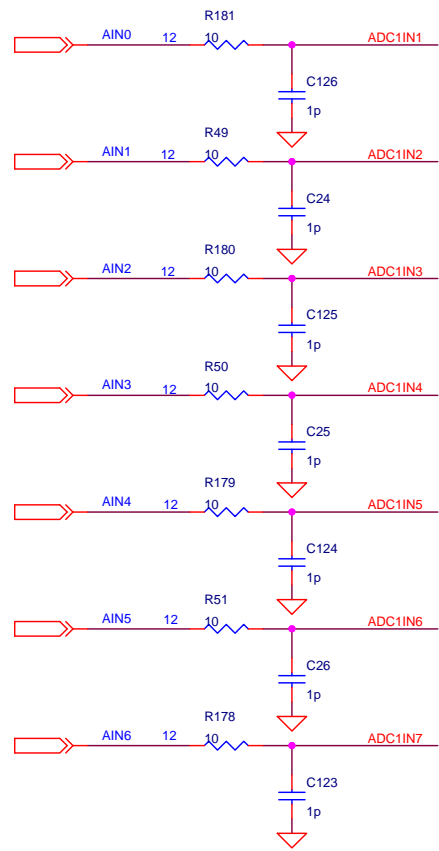
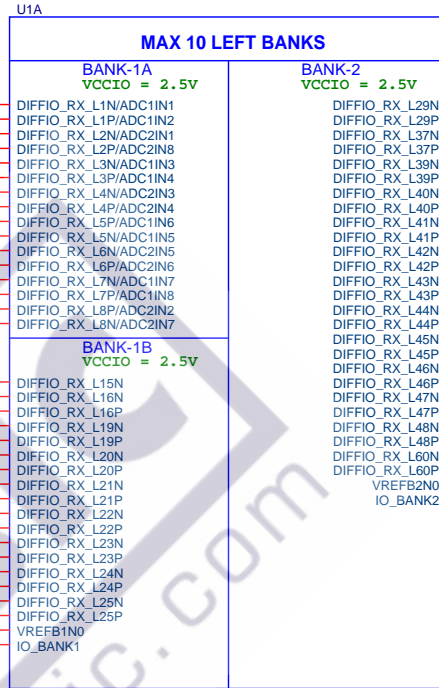
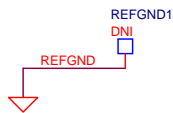
### Audio LINE-IN to MAX10 ADC



### Ethernet



### Header Analog Input



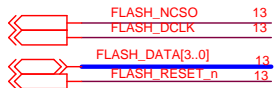
terasic Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DECA**

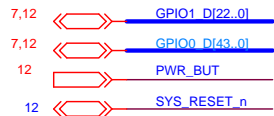
Size B	Document Number MAX 10 Bank 1, Bank 2	Rev C
--------	--	-------

Date: Wednesday, March 11, 2015 Sheet 3 of 25

**QSPI Flash**



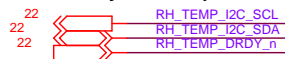
**Header GPIO**



**Temperature Sensor**



**Humidity and Temperature Sensor**



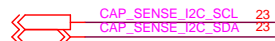
**Gesture Sensor**



**Power Monitor**



**CapSense Buttons**



**Micro SD Card**



U1B

**MAX 10 BOTTOM BANKS**

**BANK-3**  
VCCIO = 3.3V

**BANK-4**  
VCCIO = 3.3V

GPIO1_D13	Y7	DIFFIO_RX_B10N	W11	GPIO0_D35
LIGHT_I2C_SCL	Y8	DIFFIO_RX_B10P	Y11	GPIO0_D32
CAP_SENSE_I2C_SCL	AB2	DIFFIO_RX_B12N	AB10	GPIO0_D30
CAP_SENSE_I2C_SDA	AB3	DIFFIO_RX_B12P	AB11	GPIO0_D28
PMONITOR_I2C_SCL	Y3	DIFFIO_RX_B14N	AB12	GPIO0_D26
PMONITOR_ALERT	Y4	DIFFIO_RX_B14P	AB13	GPIO0_D24
	AA5	DIFFIO_RX_B17N	W12	GPIO0_D34
	AB5	DIFFIO_RX_B17P	W13	GPIO0_D33
GPIO1_D10	AB6	DIFFIO_RX_B19N	AA14	GPIO0_D23
GPIO1_D9	AB7	DIFFIO_RX_B19P	AB15	GPIO0_D18
LIGHT_I2C_SDA	AA8	DIFFIO_RX_B21N	AA15	GPIO0_D21
GPIO1_D6	AB8	DIFFIO_RX_B21P	Y16	GPIO0_D9
LIGHT_INT	AA9	DIFFIO_RX_B23N	AB16	GPIO0_D16
RH_TEMP_DRDY_n	AB9	DIFFIO_RX_B23P	AA16	GPIO0_D15
FLASH_DATA1	V4	DIFFIO_RX_B2N	AB19	GPIO0_D8
FLASH_DATA2	V5	DIFFIO_RX_B2P	AB20	GPIO0_D7
PMONITOR_I2C_SDA	Y1	DIFFIO_RX_B4N	AA19	GPIO0_D5
TEMP_SIO	Y2	DIFFIO_RX_B4P	Y18	GPIO0_D1
TEMP_SC	AA1	DIFFIO_RX_B6N	AB21	GPIO0_D6
SYS_RESET_n	AA2	DIFFIO_RX_B6P	AA20	GPIO0_D4
GPIO1_D0	Y5	DIFFIO_RX_B8N	AB17	GPIO0_D14
GPIO1_D1	Y6	DIFFIO_RX_B8P	AB18	GPIO0_D11
GPIO1_D16	W9	DIFFIO_TX_RX_B11N	V11	GPIO0_D37
FLASH_RESET_n	W10	DIFFIO_TX_RX_B11P	V12	GPIO0_D36
GPIO1_D3	W7	DIFFIO_TX_RX_B13N	R12	FLASH_DCLK
GPIO1_D4	W8	DIFFIO_TX_RX_B13P	P12	FLASH_DATA0
FLASH_NCSC0	R10	DIFFIO_TX_RX_B15N	AA11	GPIO0_D29
FLASH_DATA3	P10	DIFFIO_TX_RX_B15P	AA12	GPIO0_D27
GPIO1_D12	AA6	DIFFIO_TX_RX_B16N	V13	GPIO0_D38
GPIO1_D11	AA7	DIFFIO_TX_RX_B16P	W14	GPIO0_D41
GPIO1_D17	W5	DIFFIO_TX_RX_B1N	R13	GPIO0_D43
GPIO1_D2	W6	DIFFIO_TX_RX_B1P	P13	SD_SEL
RH_TEMP_I2C_SCL	Y10	DIFFIO_TX_RX_B22N	Y13	GPIO0_D31
RH_TEMP_I2C_SDA	AA10	DIFFIO_TX_RX_B22P	Y14	GPIO0_D20
PWR_BUT1	U6	DIFFIO_TX_RX_B3N	V14	GPIO0_D39
GPIO1_D15	U7	DIFFIO_TX_RX_B3P	W15	GPIO0_D19
GPIO1_D19	W4	DIFFIO_TX_RX_B5N	U15	GPIO0_D42
GPIO1_D22	W3	DIFFIO_TX_RX_B5P	V16	GPIO0_D10
GPIO1_D7	V7	DIFFIO_TX_RX_B7N	AA17	GPIO0_D3
GPIO1_D5	V8	DIFFIO_TX_RX_B7P	Y17	GPIO0_D40
GPIO1_D18	R9	DIFFIO_TX_RX_B9N	V15	GPIO0_D12
GPIO1_D20	P9	DIFFIO_TX_RX_B9P	W16	GPIO0_D17
	AA3	VREFB3N0	Y19	GPIO0_D2
TEMP_CS_n	AB4	IO_BANK3	W18	GPIO0_D0
		IO_BANK4	AA13	GPIO0_D25
			AB14	GPIO0_D22
				VREFB4N0
				IO_BANK4

10M50DAF484C6GES

terasic Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

**Title**  
DECA

**Size** B    **Document Number** MAX 10 Bank 3 & 4    **Rev** C

**Date:** Wednesday, March 11, 2015    **Sheet** 4 of 25

VCC1P5\_DDR3

U1C

MAX 10 RIGHT BANKS

BANK-5  
VCCIO = 1.5V

BANK-6  
VCCIO = 1.5V

DDR3_RESET_n	U19	DIFFIO_RX_R19N
DDR3_A6	V18	DIFFIO_RX_R19P
	U18	DIFFIO_RX_R19P/RUP
	U17	DIFFIO_RX_R1N/RDN
DDR3_A9	W22	DIFFIO_RX_R20N
DDR3_A11	Y22	DIFFIO_RX_R20P
DDR3_A14	W20	DIFFIO_RX_R21N
DDR3_BA1	W19	DIFFIO_RX_R21P
DDR3_A4	Y21	DIFFIO_RX_R22N
DDR3_A8	Y20	DIFFIO_RX_R22P
DDR3_A7	U20	DIFFIO_RX_R23N
DDR3_A1	V20	DIFFIO_RX_R23P
DDR3_A13	V22	DIFFIO_RX_R24N
DDR3_A2	V21	DIFFIO_RX_R24P
AUDIO_BCLK	R14	DIFFIO_RX_R24P
AUDIO_WCLK	R15	DIFFIO_RX_R25N/DQ1R
SD_D0_DIR	T22	DIFFIO_RX_R25P/DQ1R
SD_CMD	T21	DIFFIO_RX_R26N
SD_DAT1	T18	DIFFIO_RX_R26P
SD_DAT2	T19	DIFFIO_RX_R27N/DM1R
SD_DAT3	R20	DIFFIO_RX_R27P/DQ1R
SD_CLK	T20	DIFFIO_RX_R28N/DQ1R
SD_CMD_DIR	U22	DIFFIO_RX_R28P/DQ1R
SD_DT23_DIR	U21	DIFFIO_RX_R29N
	AA22	DIFFIO_RX_R29P
	AA21	DIFFIO_RX_R2N
AUDIO_MCLK	P14	DIFFIO_RX_R2P
AUDIO_DIN_MFP1	P15	DIFFIO_RX_R30N/DQ1R
AUDIO_SPI_SELECT	N22	DIFFIO_RX_R30P/DQ1R
AUDIO_SDA_MOSI	P21	DIFFIO_RX_R31N
AUDIO_DOUT_MFP2	P18	DIFFIO_RX_R31P
SD_DAT0	R18	DIFFIO_RX_R32N/DQSN1R
AUDIO_SCL_SS_n	P20	DIFFIO_RX_R32P/DQSN1R
AUDIO_SCLK_MFP3	P19	DIFFIO_RX_R33N/DQ1R
	L22	DIFFIO_RX_R33P/DQ1R
AUDIO_RESET_n	M21	DIFFIO_RX_R34N
AUDIO_GPIO_MFP5	M22	DIFFIO_RX_R34P
AUDIO_MISO_MFP4	N21	DIFFIO_RX_R35N
AUDIO_SPI_SELECT	N21	DIFFIO_RX_R35P
DDR3_VREF	P22	DIFFIO_RX_R35P
SD_FB_CLK	R22	VREFB5N0
		IO_BANK5

10M50DAF484C6GES

DDR3_CK_p	13
DDR3_CK_n	13
DDR3_CKE	13
DDR3_RESET_n	13
DDR3_WE_n	13
DDR3_RAS_n	13
DDR3_CAS_n	13
DDR3_CS_n	13
DDR3_ODT	13

13	DDR3_A[14..0]	
13	DDR3_DM[1..0]	
13	DDR3_BA[2..0]	
	DDR3_DQ[15..0]	13
	DDR3_DQS_p[1..0]	7,13
	DDR3_DQS_n[1..0]	7,13

Micro SD Card

14	SD_DAT[3..0]
14	SD_CMD
14	SD_CLK
14	SD_D0_DIR
14	SD_D123_DIR
14	SD_CMD_DIR
14	SD_FB_CLK

Audio CODEC Interface

17	AUDIO_MCLK
17	AUDIO_BCLK
17	AUDIO_WCLK
17	AUDIO_DIN_MFP1
17	AUDIO_DOUT_MFP2

Audio Control Interface

17	AUDIO_SCLK_MFP3
17	AUDIO_SCL_SS_n
17	AUDIO_SDA_MOSI
17	AUDIO_MISO_MFP4
17	AUDIO_SPI_SELECT
17	AUDIO_RESET_n
17	AUDIO_GPIO_MFP5

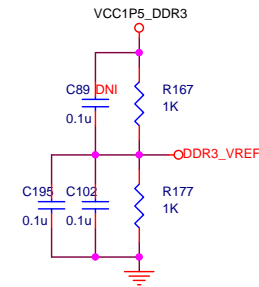
SWITCH

23	SW[1..0]
----	----------

KEY

23	KEY[1..0]
----	-----------

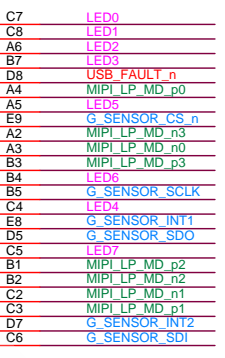
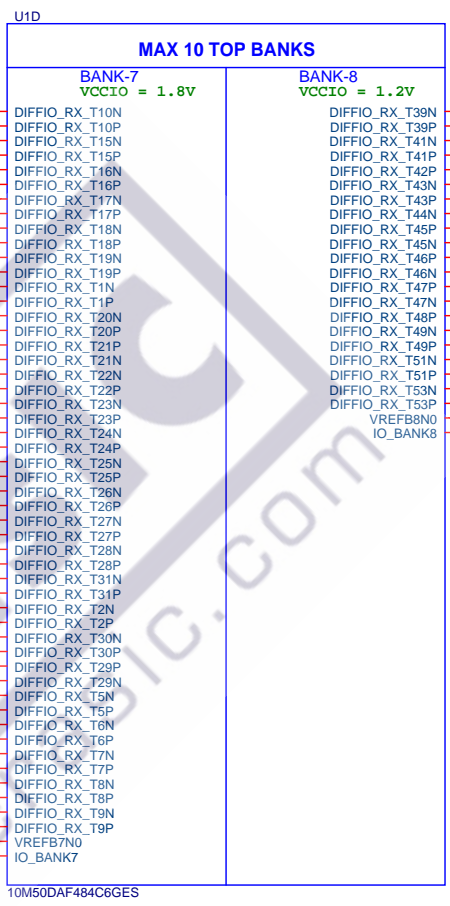
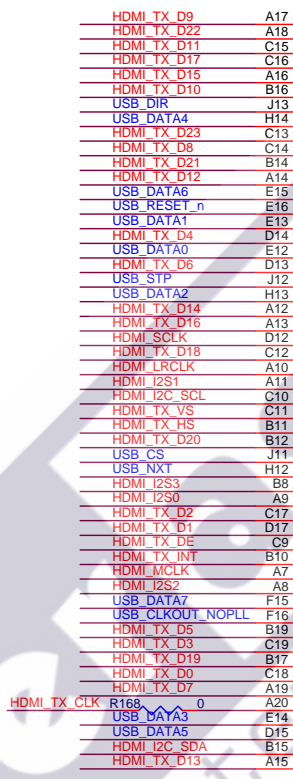
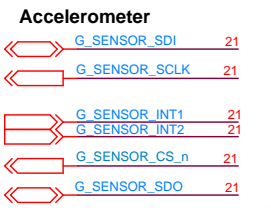
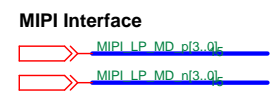
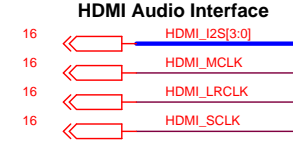
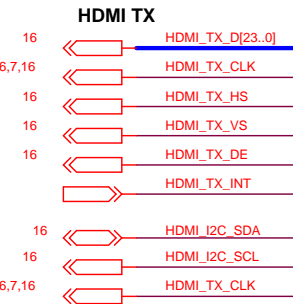
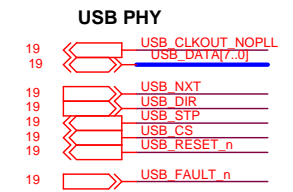
H21	KEY0
H22	KEY1
J21	SW0
J22	SW1
G19	
G20	
F22	DDR3_CS_n
G22	DDR3_ODT
M14	DDR3_DQ5
M15	DDR3_DQ3
E21	DDR3_A0
E22	DDR3_WE_n
N19	DDR3_DM0
N18	DDR3_A12
M20	DDR3_DQ6
N20	DDR3_DQ7
F20	
F21	DDR3_R48N
C22	DDR3_A10
D22	DDR3_RAS_n
L18	DDR3_DQ2
M18	DDR3_DQ4
L20	DDR3_DQ0
L19	DDR3_DQ1
F18	
E19	
E20	DDR3_CAS_n
F19	DDR3_BA2
K15	DDR3_DQS_n1
K14	DDR3_DQS_p1
D19	DDR3_BA0
C20	DDR3_A3
J18	DDR3_DQ10
K18	DDR3_DQ9
K20	DDR3_DQ11
K19	DDR3_DQ8
E17	
F17	
B21	
B22	DDR3_CKE
J15	DDR3_DM1
J14	DDR3_A5
A21	
B20	
H18	DDR3_DQ12
H19	DDR3_DQ15
H20	DDR3_DQ14
J20	DDR3_DQ13
E18	DDR3_CK_n
D18	DDR3_CK_p
D21	DDR3_VREF
C21	

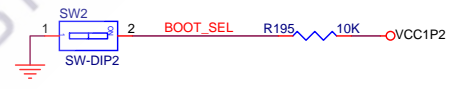
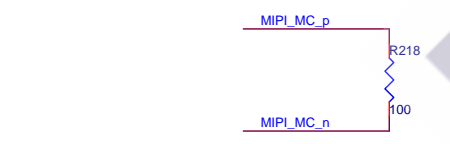
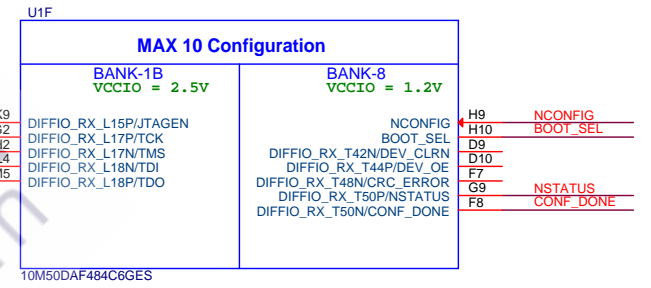
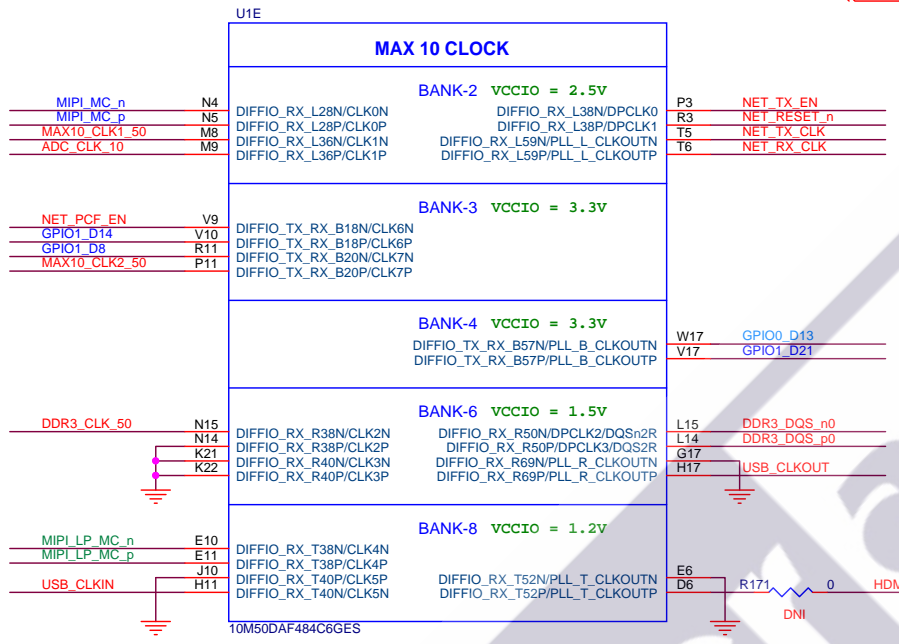
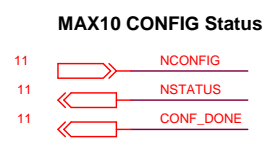
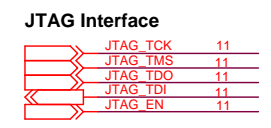
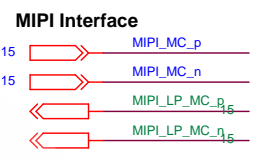
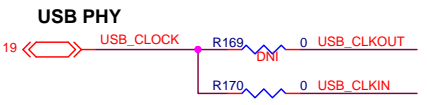
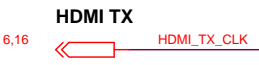
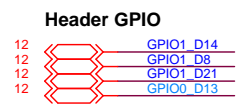
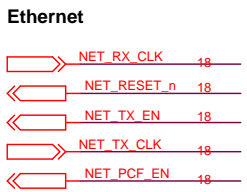
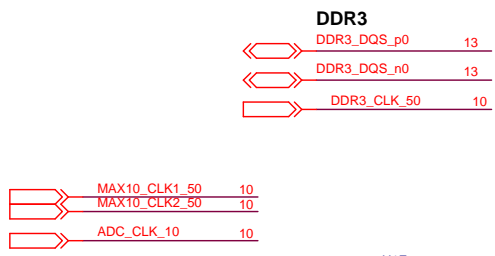


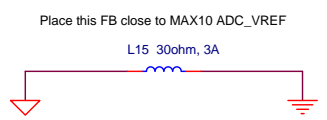
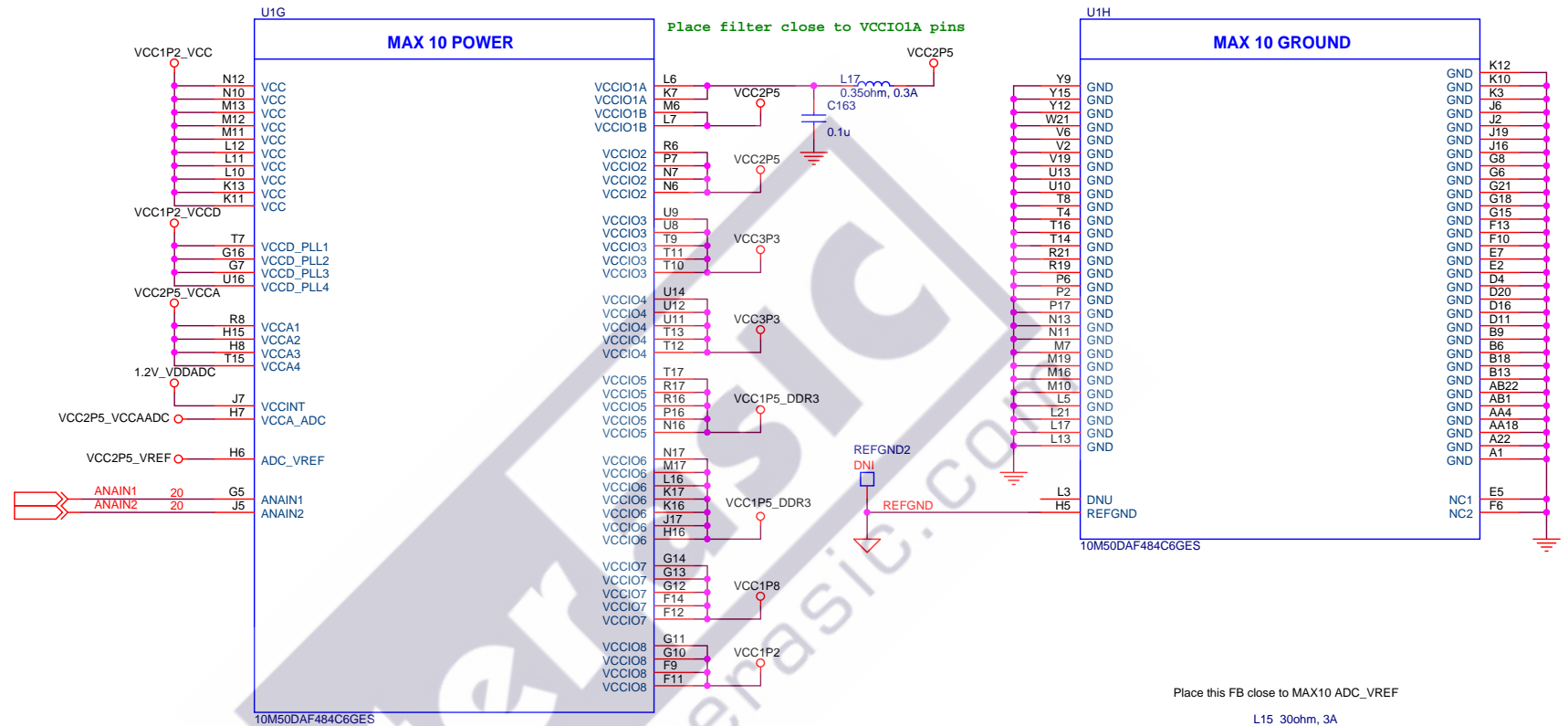
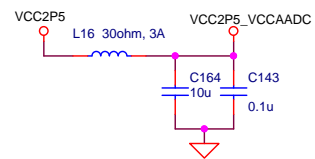
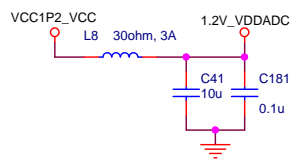
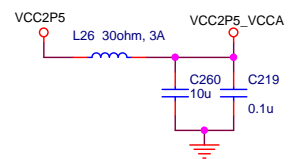
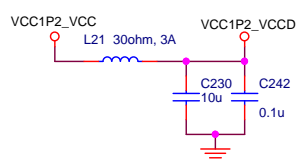
terasic Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: **DECA**

Size: B	Document Number: MAX 10 Bank 5 & 6	Rev: C
Date: Wednesday, March 11, 2015	Sheet: 5	of 25

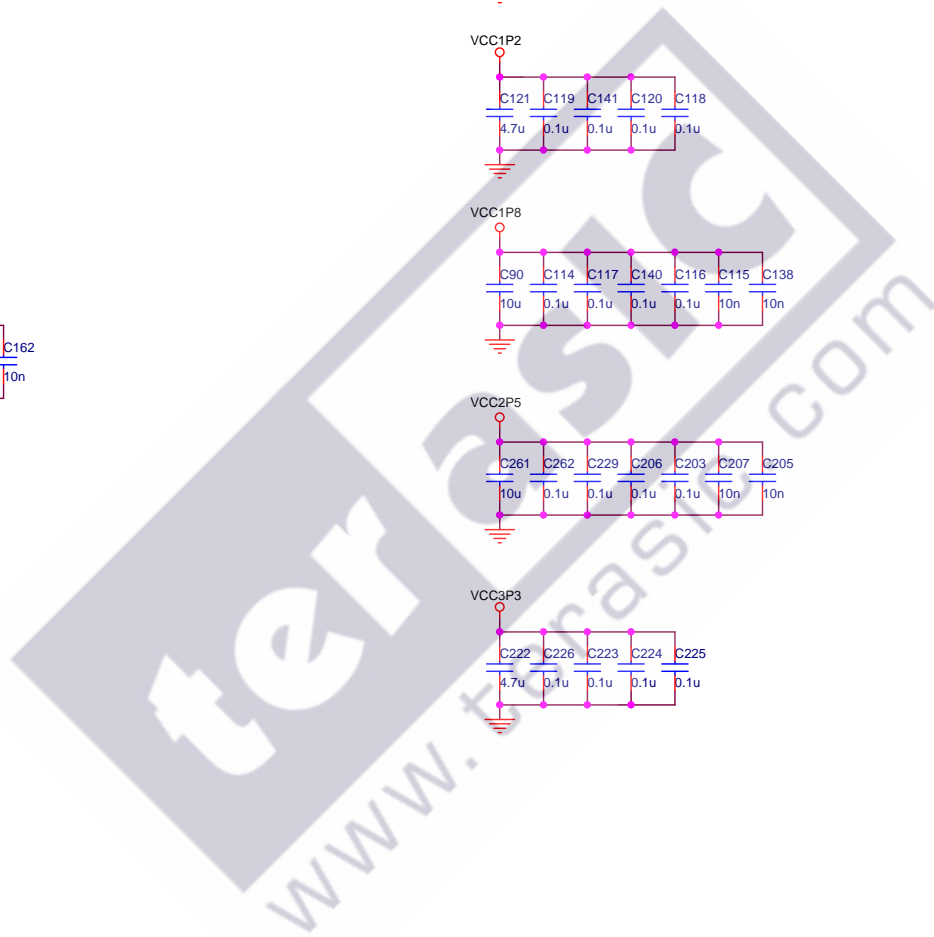
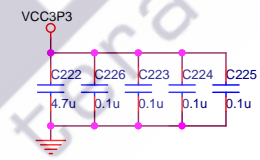
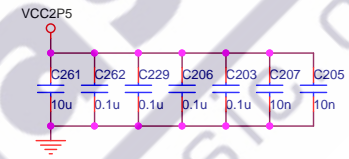
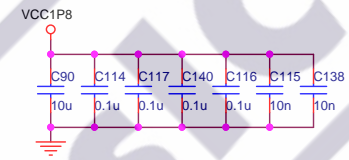
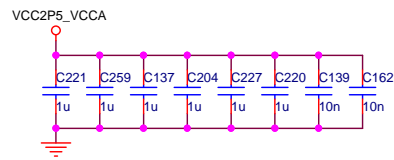
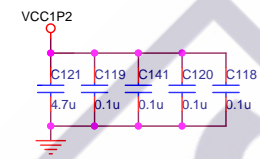
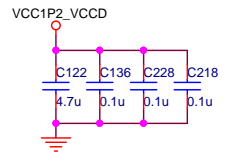
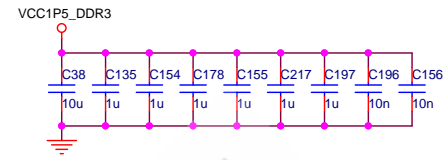
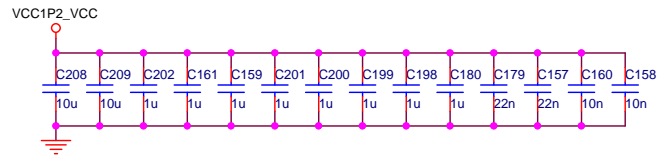





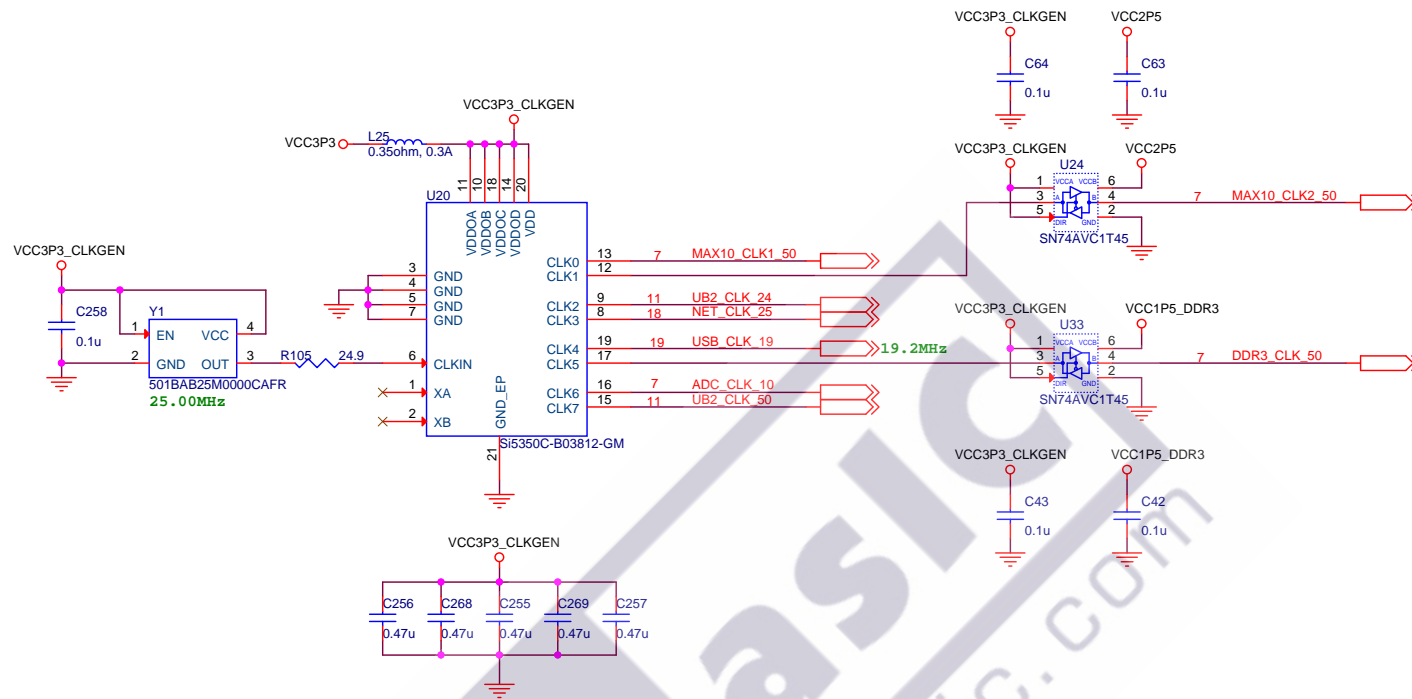



Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DECA		
Size	Document Number	Rev
B	MAX10 Power & GND	C
Date:	Wednesday, March 11, 2015	Sheet 8 of 25

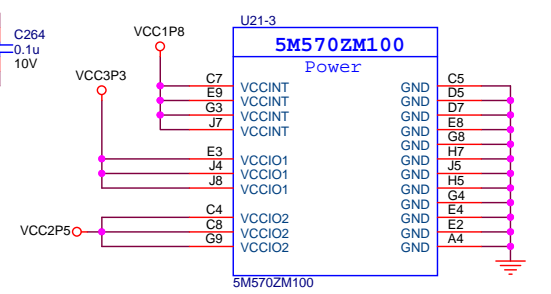
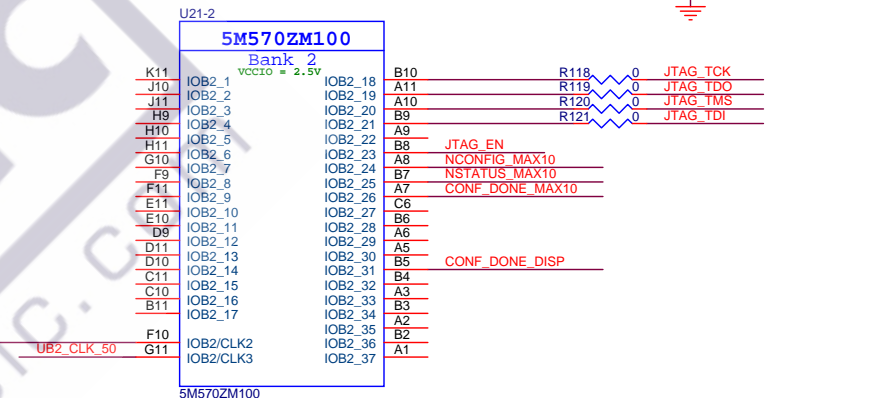
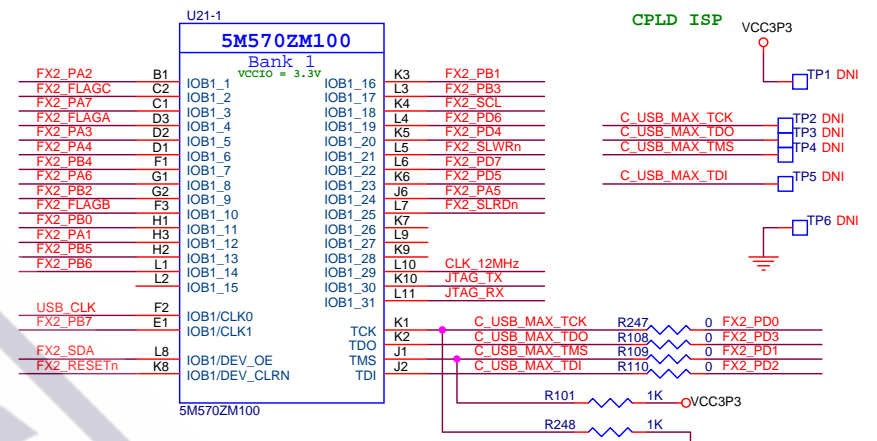
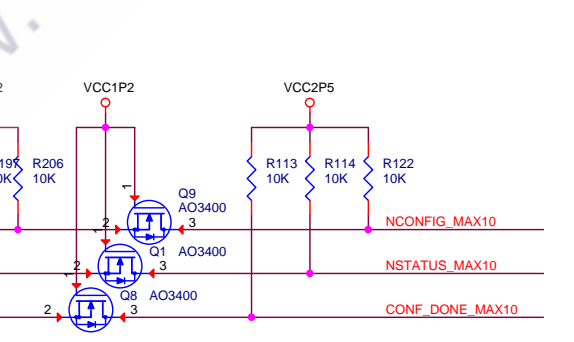
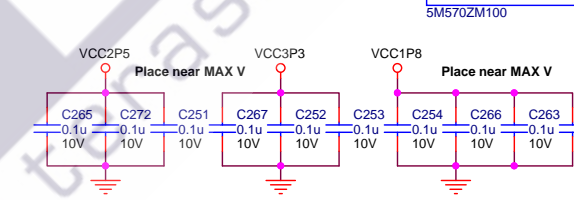
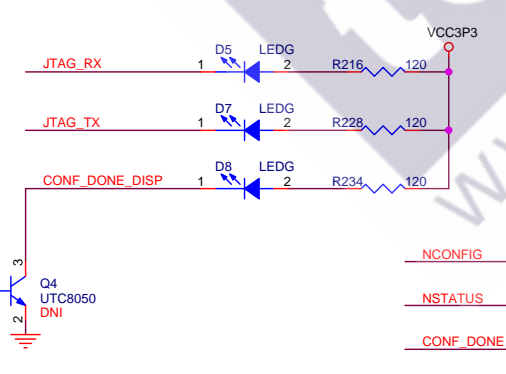
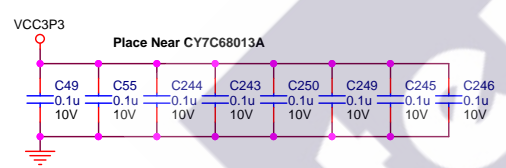
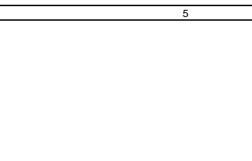
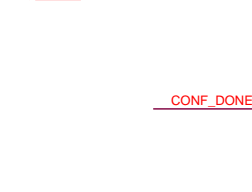
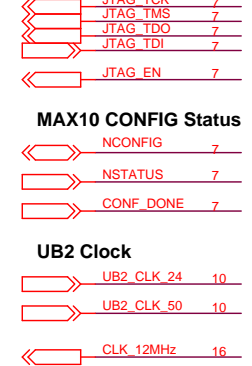
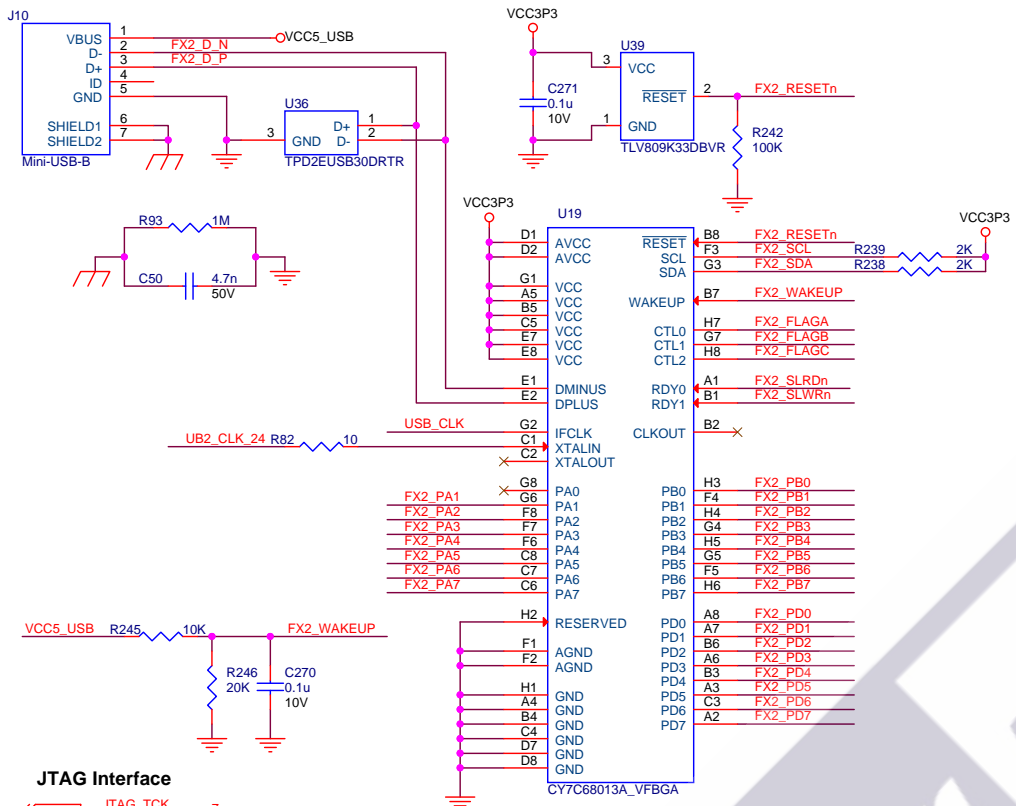




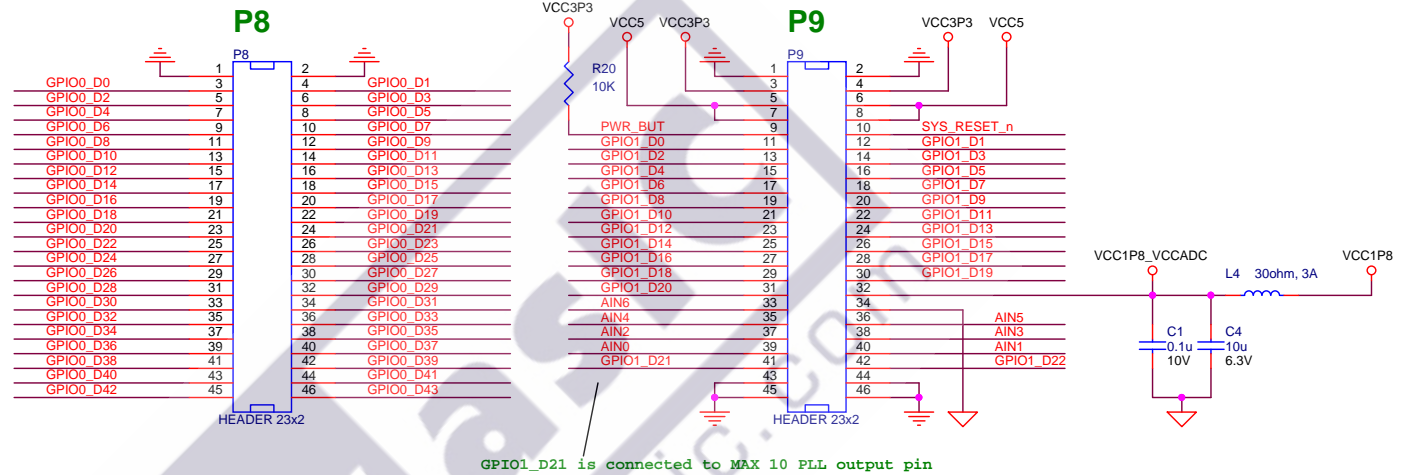
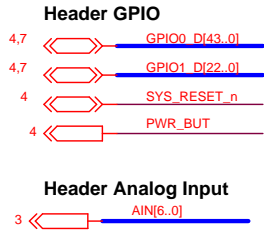
 Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	MAX10 Decoupling	C
Date:	Wednesday, March 11, 2015	Sheet 9 of 25



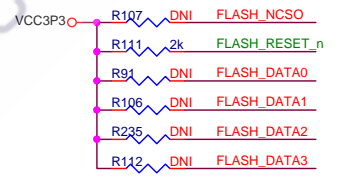
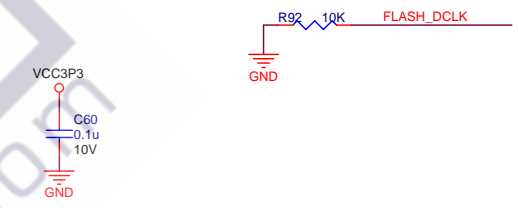
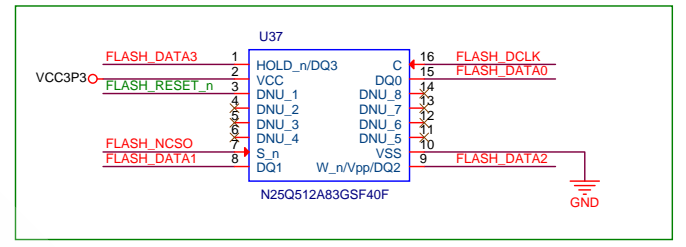
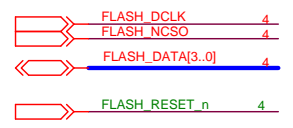
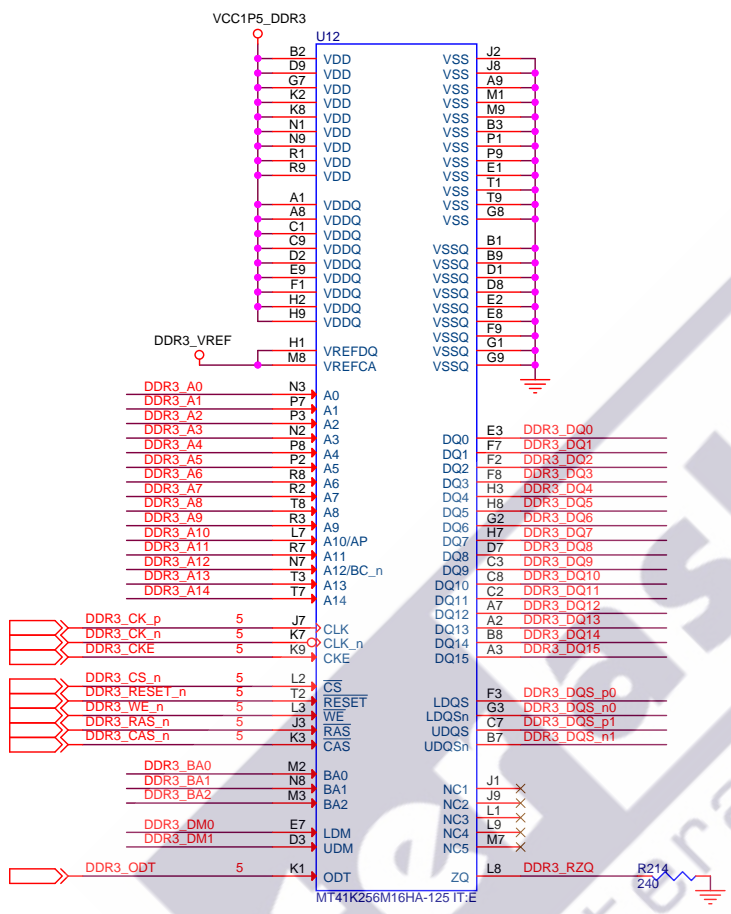
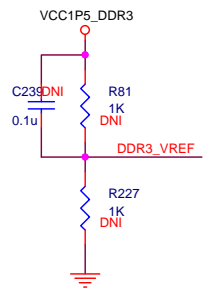
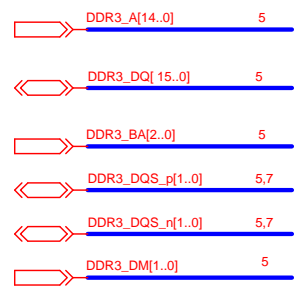
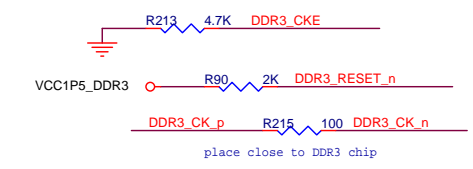
 Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	Oscillator, Clock Generator	C
Date:	Wednesday, March 11, 2015	Sheet 10 of 25



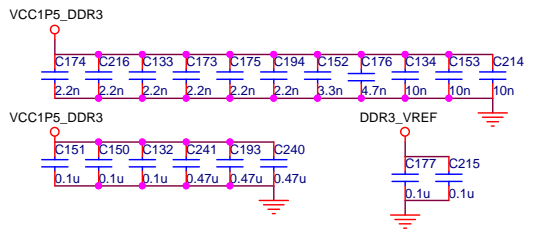
Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	USB Blaster II	C
Date:	Friday, March 13, 2015	Sheet 11 of 25



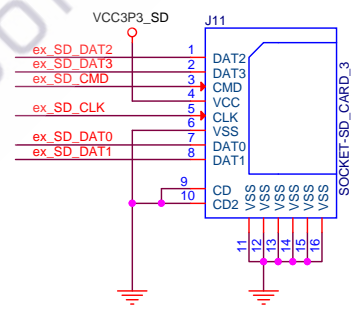
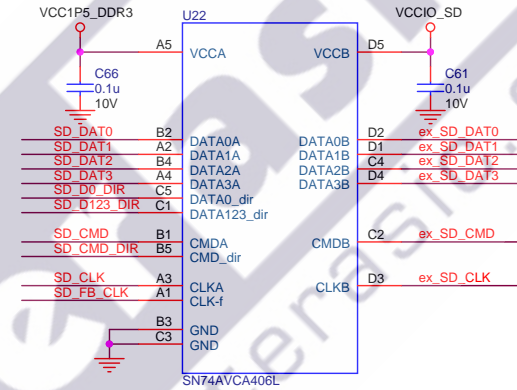
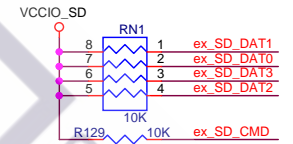
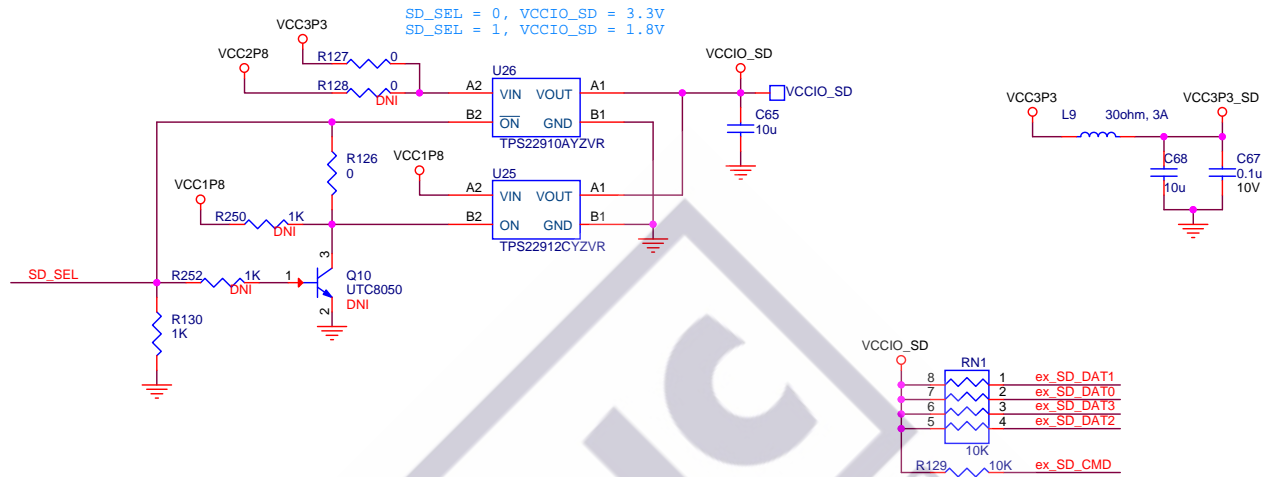
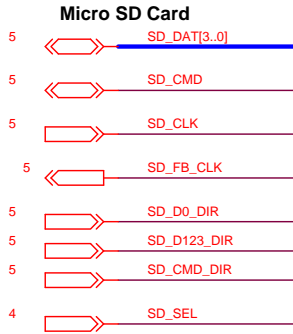
Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	Expansion Headers - BBB Headers	C
Date:	Wednesday, March 11, 2015	Sheet 12 of 25



Note: place a pull down resistor on the FLASH\_DCLK wire at the Master



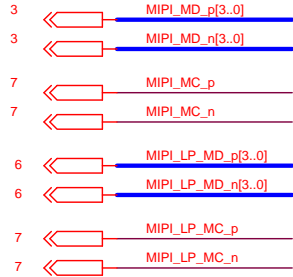
Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DECA		
Size	Document Number	Rev
B	DDR3 SDRAM, QSPI Flash	C
Date:	Wednesday, March 11, 2015	Sheet 13 of 25



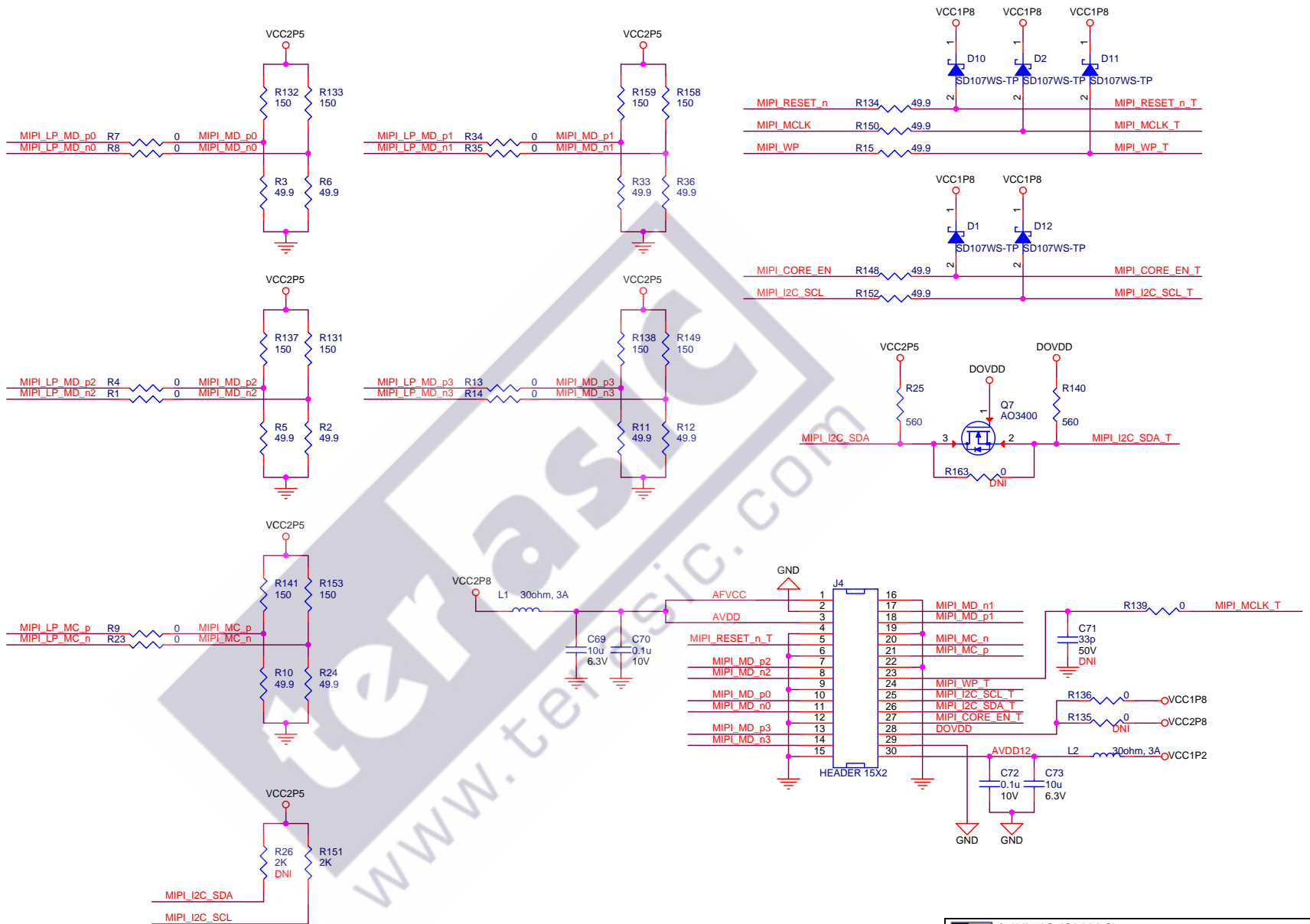
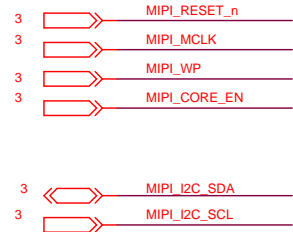
Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title		
<b>DECA</b>		
Size B	Document Number SD Card	Rev C
Date:	Wednesday, March 11, 2015	Sheet 14 of 25

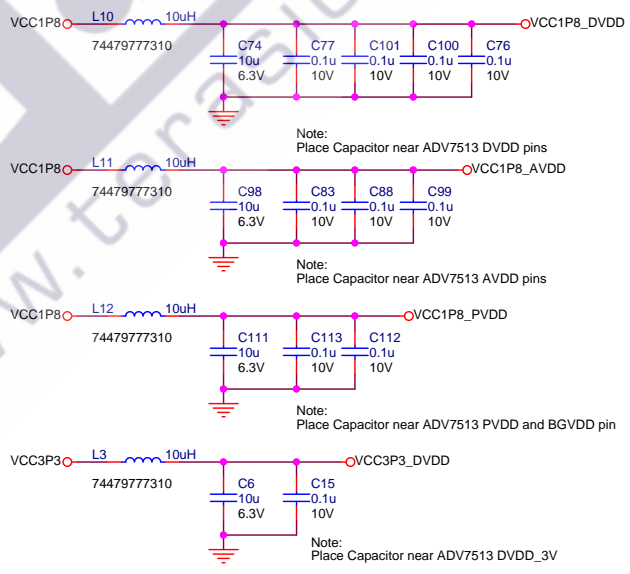
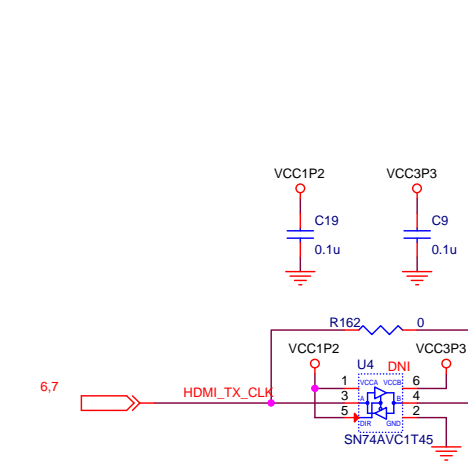
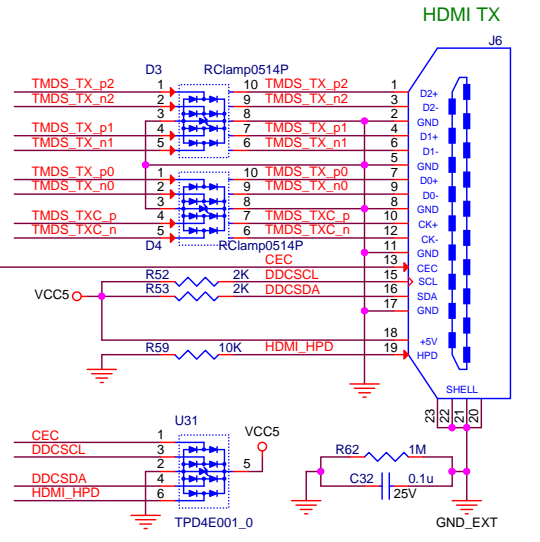
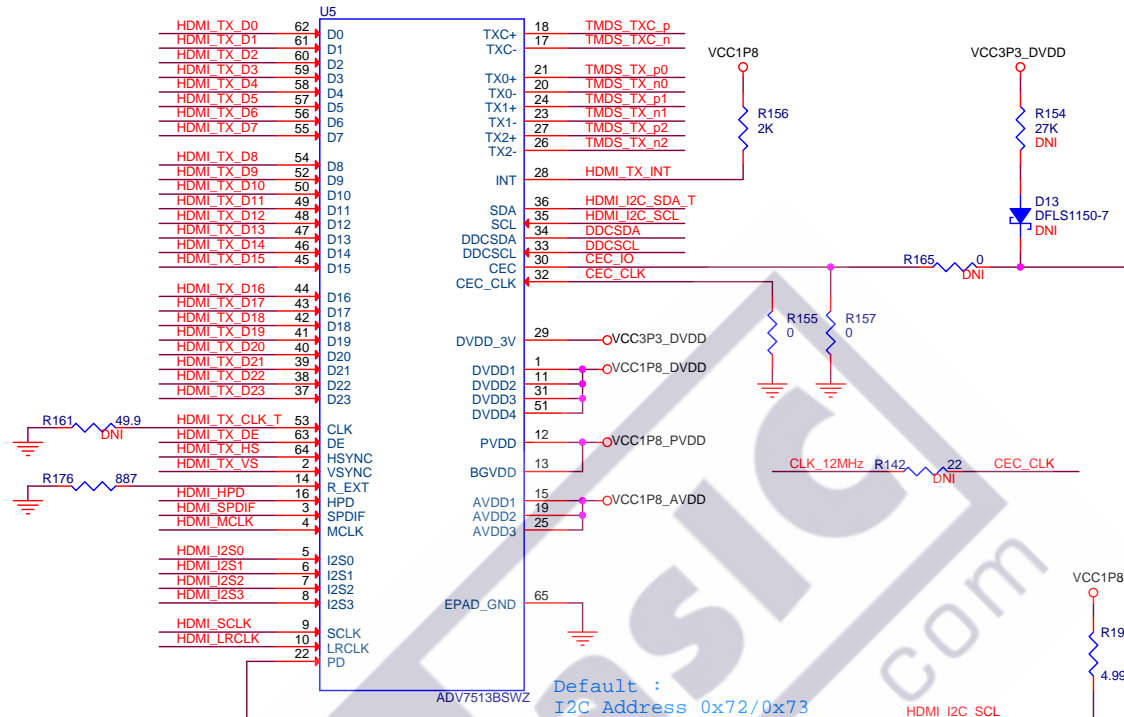
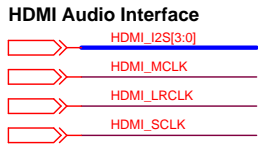
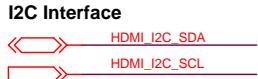
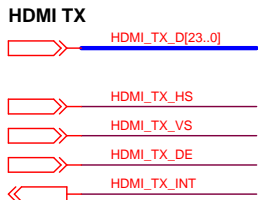
**MIPI Interface**



**MIPI Control Interface**

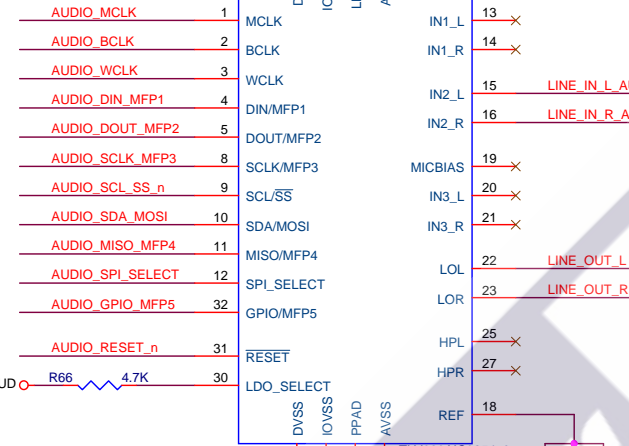
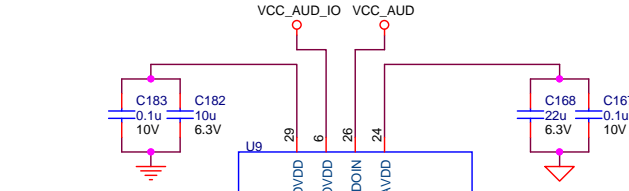
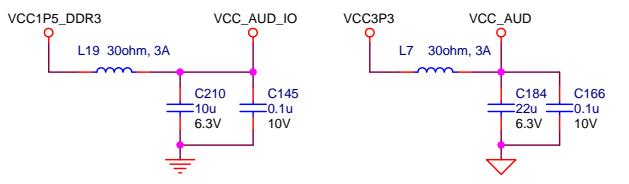
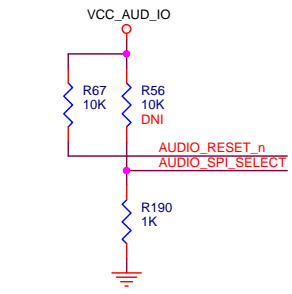
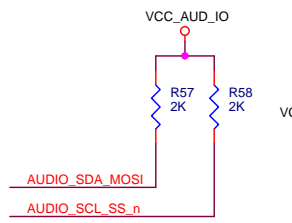
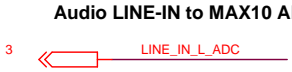
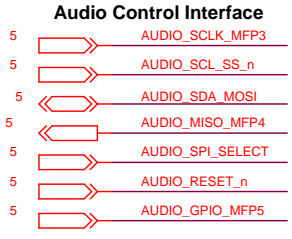
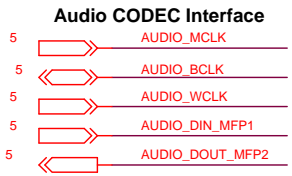


Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	MIPI Interface	C
Date:	Thursday, March 19, 2015	Sheet 15 of 25

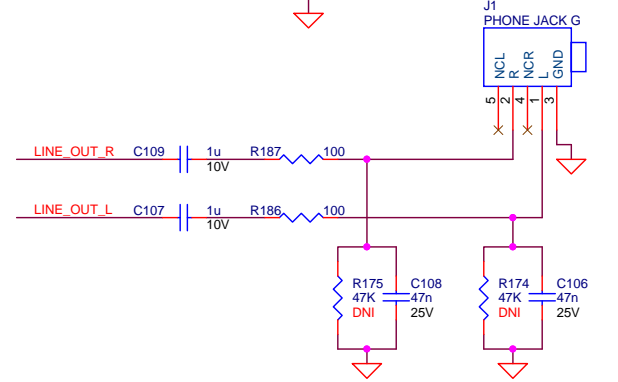
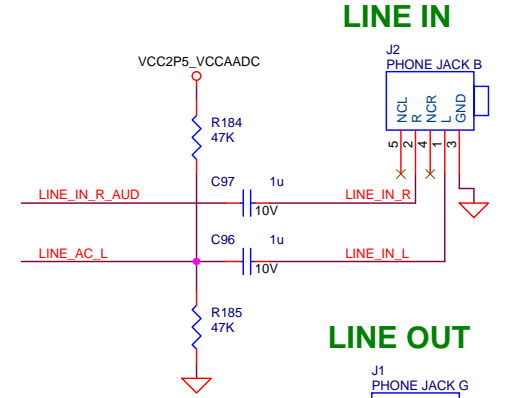
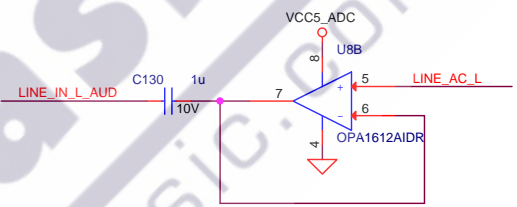
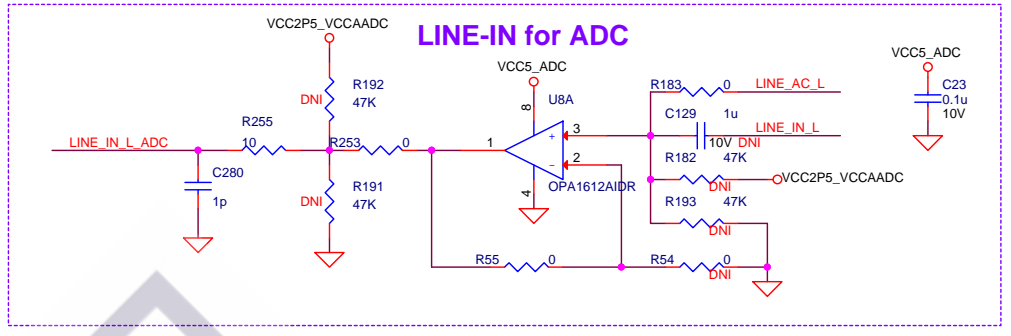
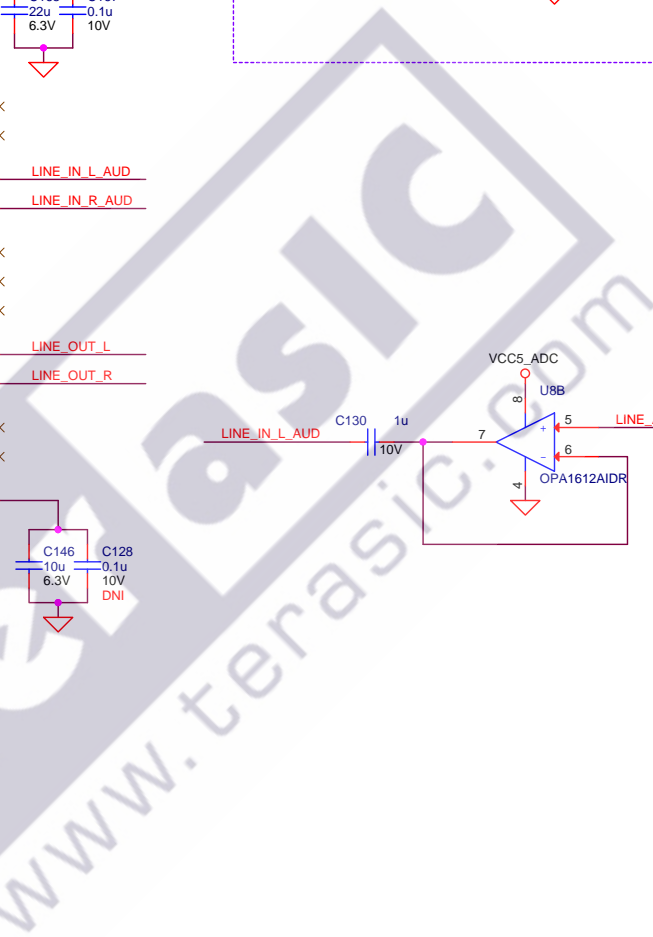


Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	HDMI TX	C
Date:	Thursday, March 19, 2015	Sheet 16 of 25

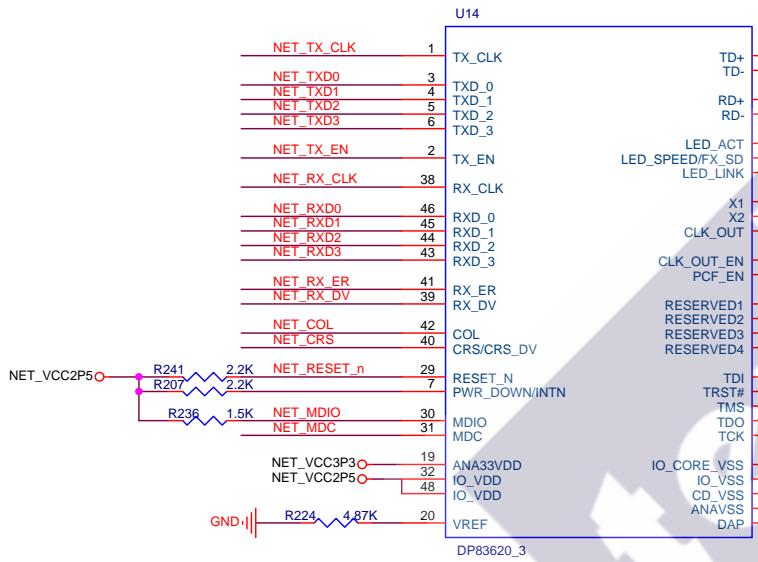
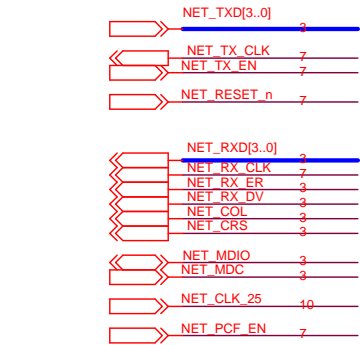




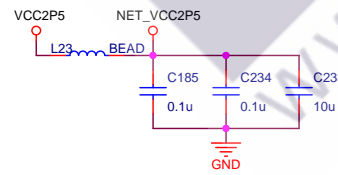
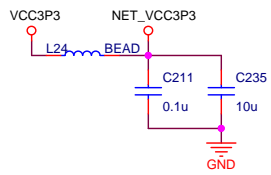
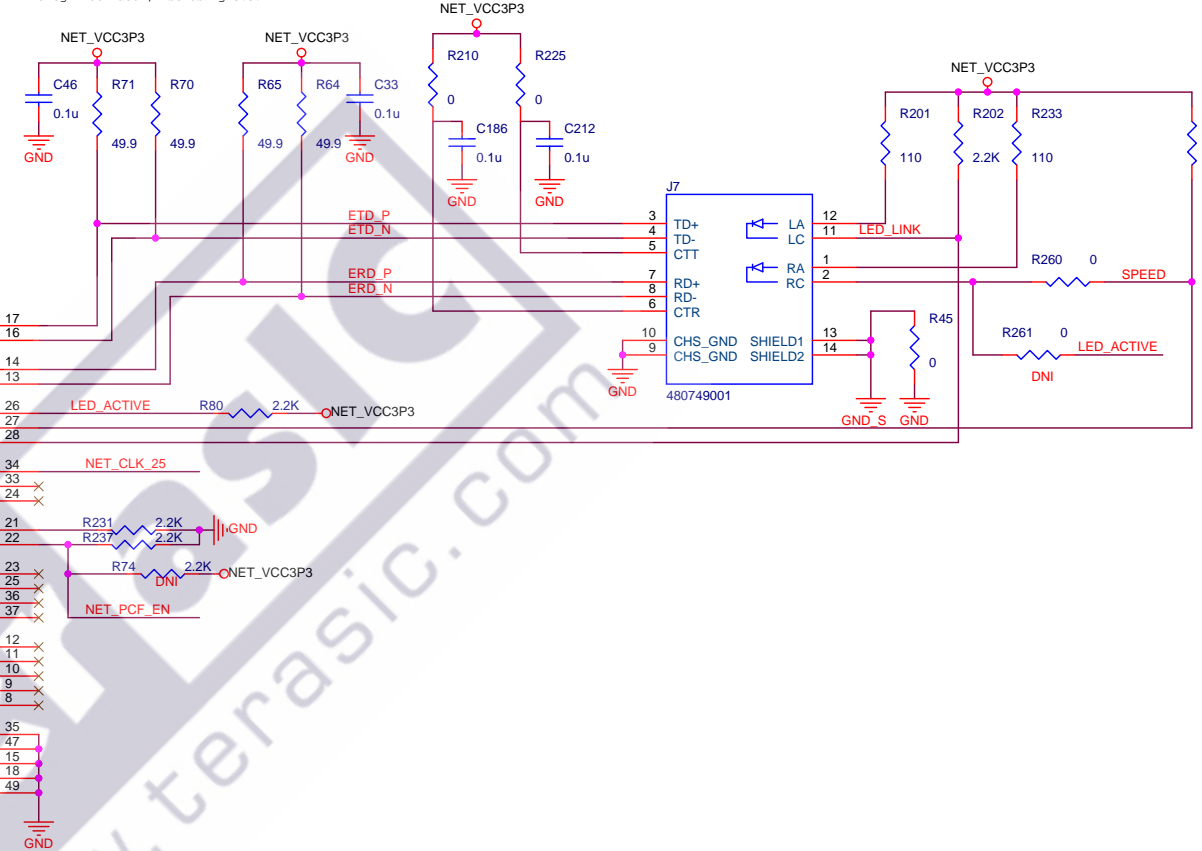
Default :  
I2C Address 0x30/31



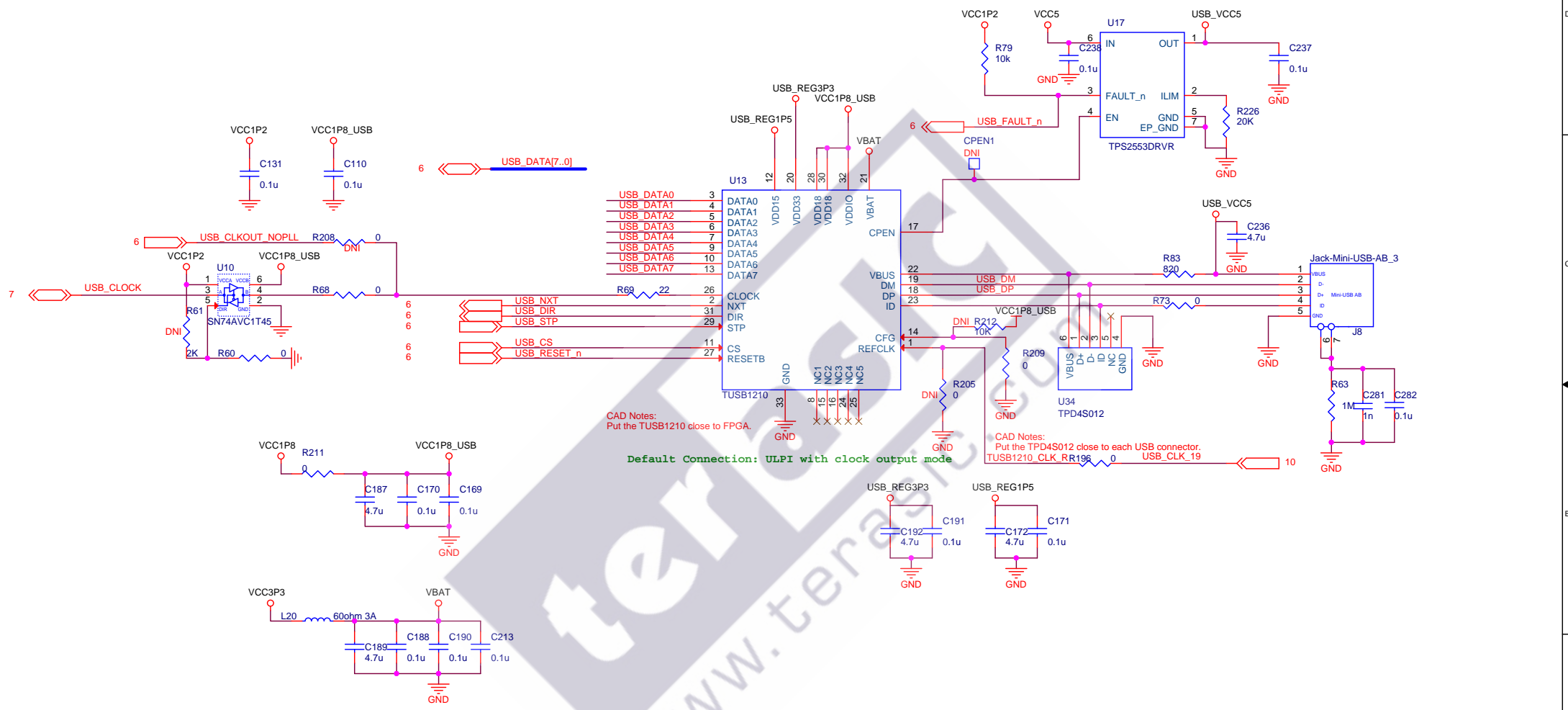
Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.			
Title			
DECA			
Size	Document Number		Rev
B	Audio CODEC		C
Date:	Friday, March 13, 2015	Sheet	17 of 25



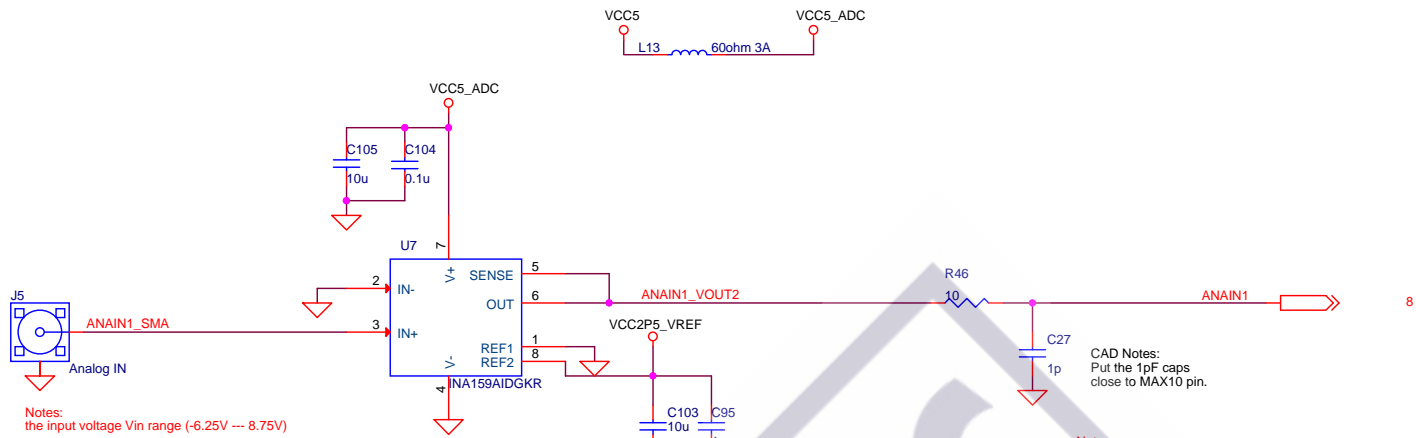
Analog interface , so using 3.3v



Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	Ethernet	C
Date:	Wednesday, March 11, 2015	Sheet 18 of 25



Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	USB PHY	C
Date:	Thursday, March 19, 2015	Sheet 19 of 25

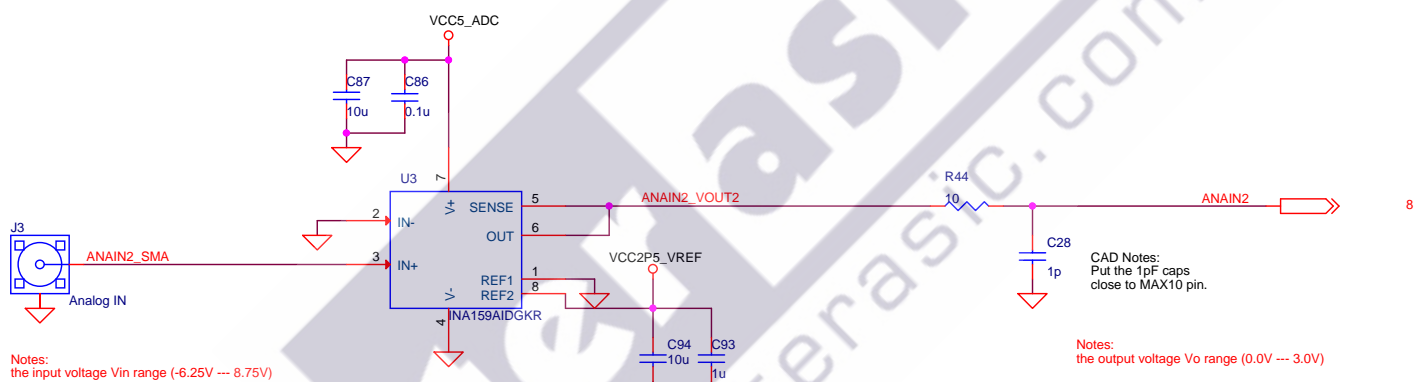


Notes:  
the input voltage  $V_{in}$  range (-6.25V --- 8.75V)

Notes:  
the output voltage  $V_o$  range (0.0V --- 3.0V)

Notes:  
Amplifier output voltage  $V_o = (6.25 + V_{in})/5$

CAD Notes:  
Put the 1pF caps  
close to MAX10 pin.

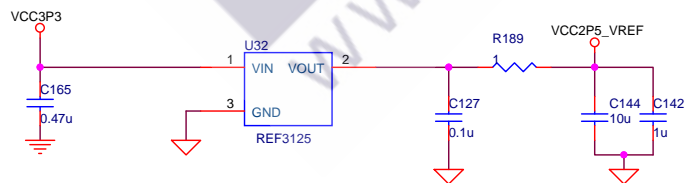


Notes:  
the input voltage  $V_{in}$  range (-6.25V --- 8.75V)

Notes:  
the output voltage  $V_o$  range (0.0V --- 3.0V)

Notes:  
Amplifier output voltage  $V_o = (6.25 + V_{in})/5$

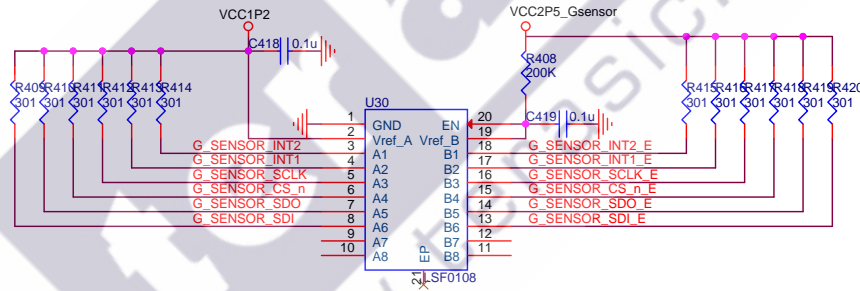
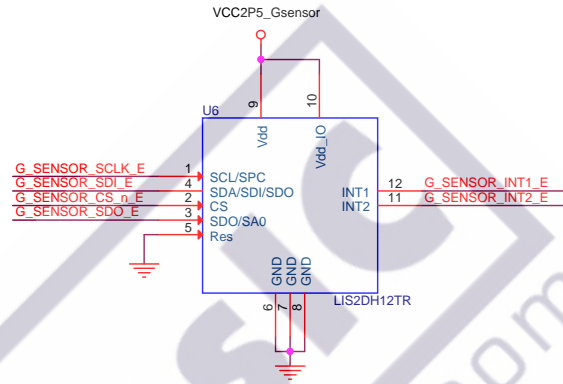
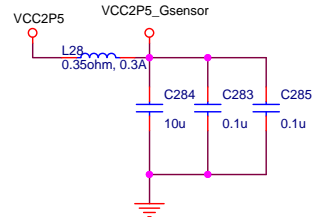
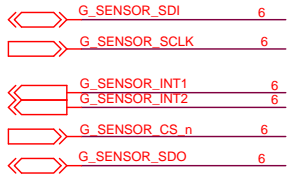
CAD Notes:  
Put the 1pF caps  
close to MAX10 pin.



Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
DECA		
Size	Document Number	Rev
B	SMA Connectors & Difference Amplifier	C
Date:	Monday, March 16, 2015	Sheet 20 of 25

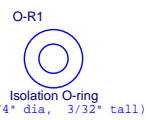
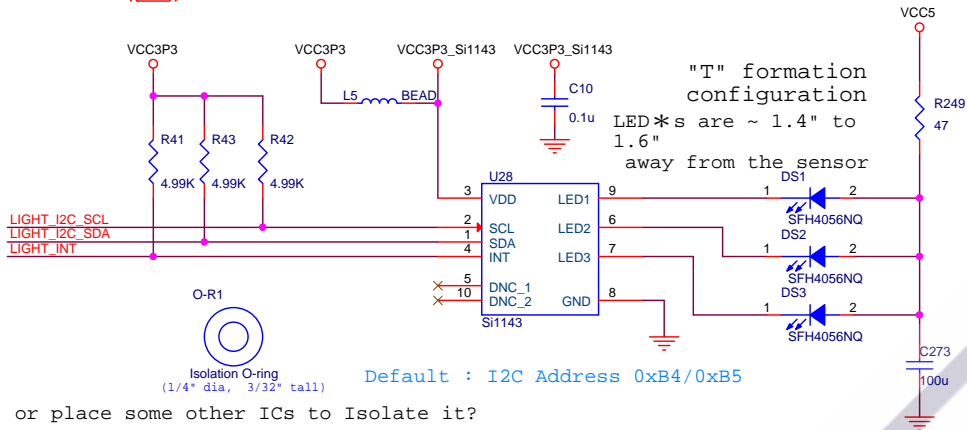
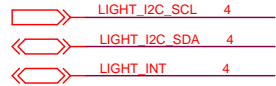
# Digital Gsensor

## Accelerometer



Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	Accelerometer	C
Date:	Thursday, March 19, 2015	Sheet 21 of 25

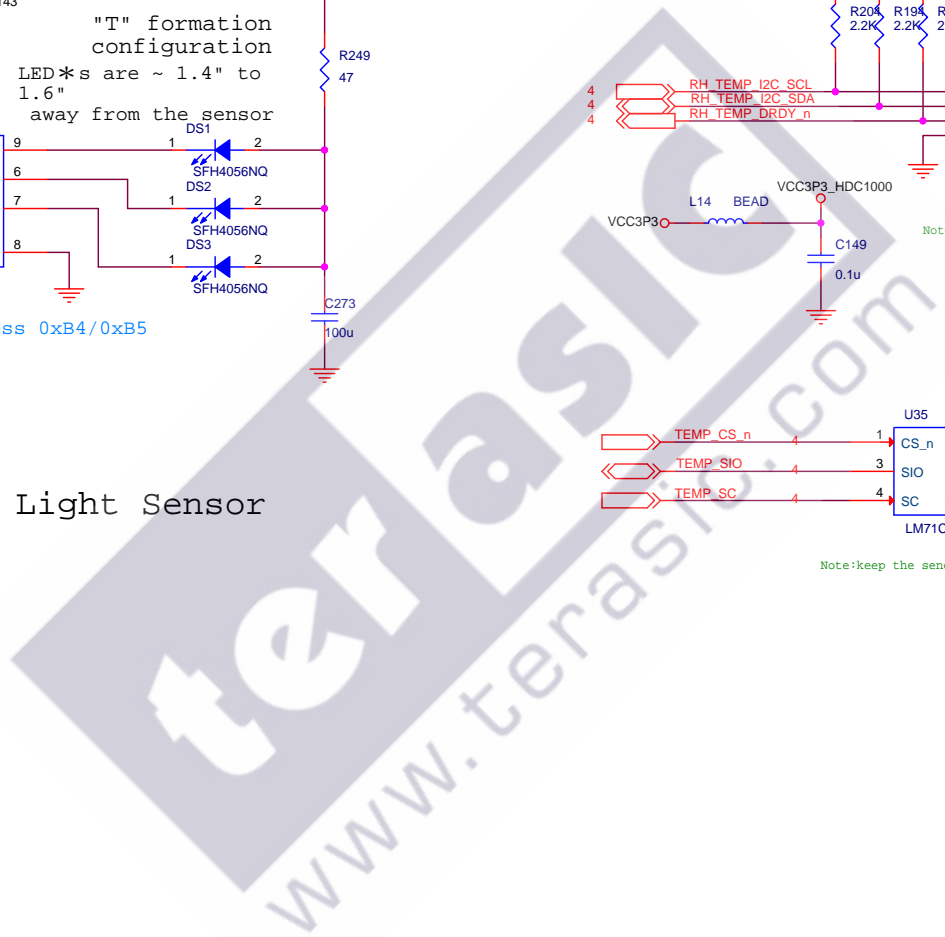
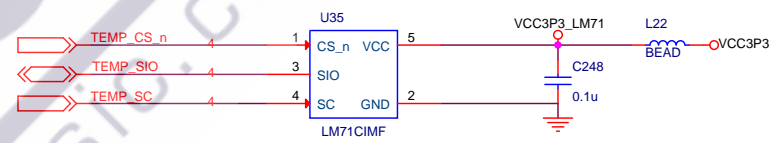
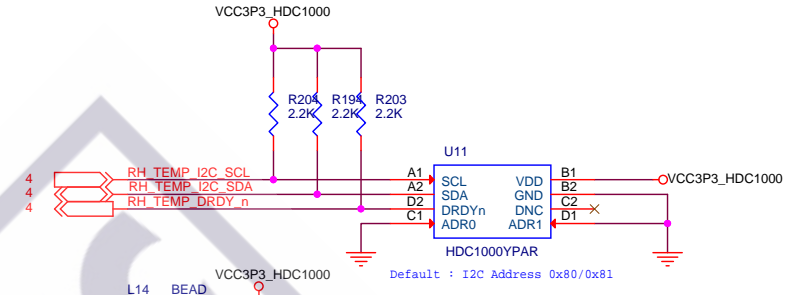
**Si1143**



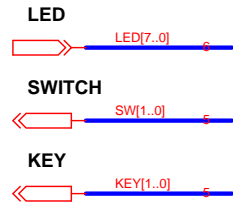
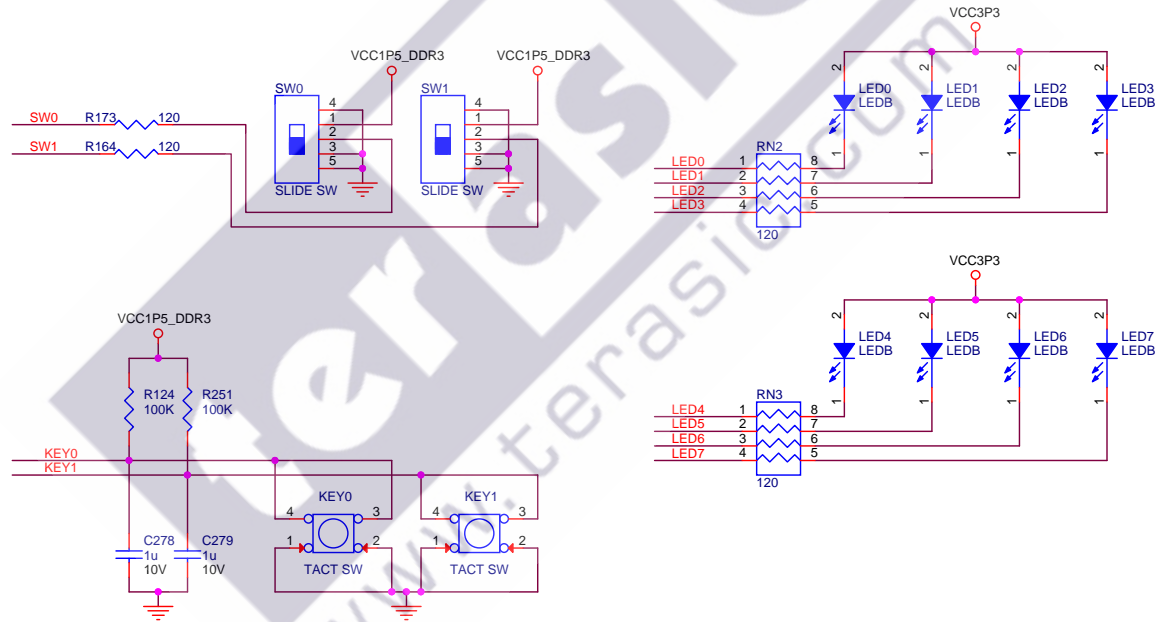
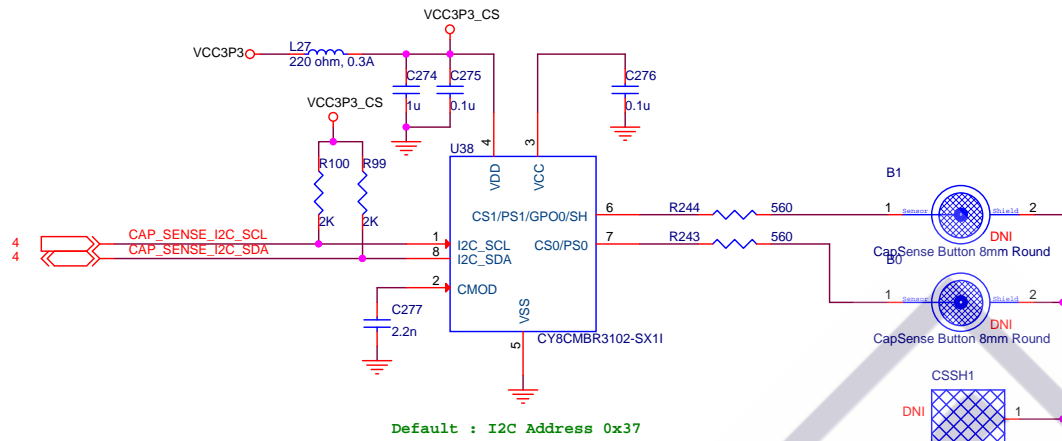
Default : I2C Address 0xB4/0xB5

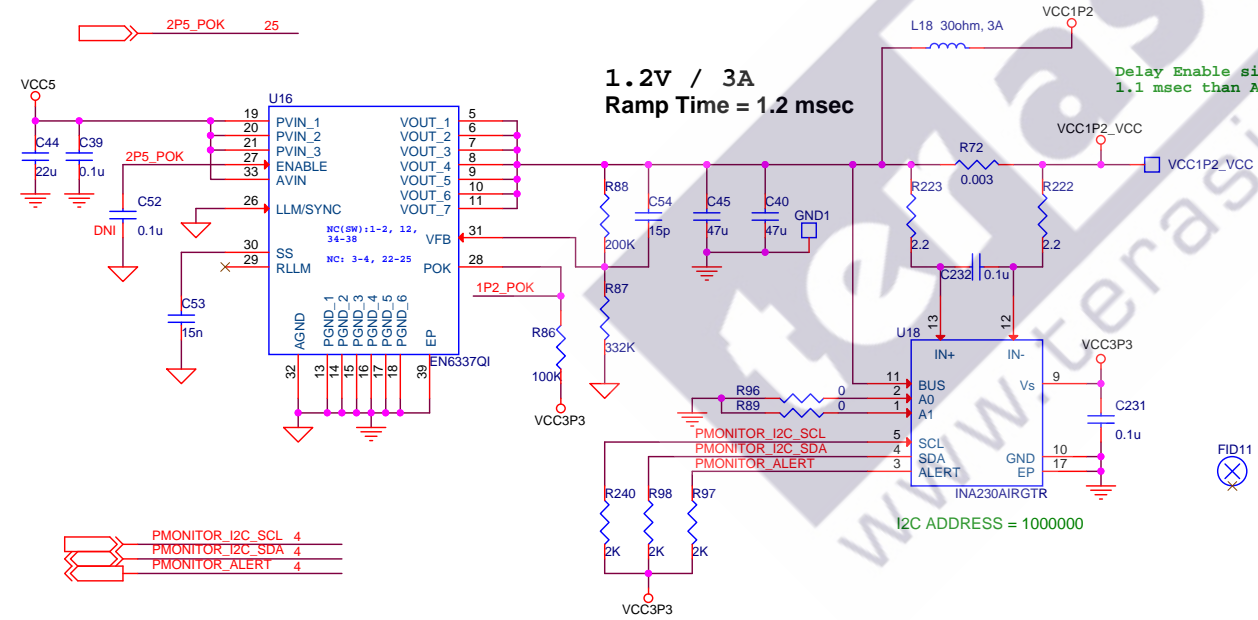
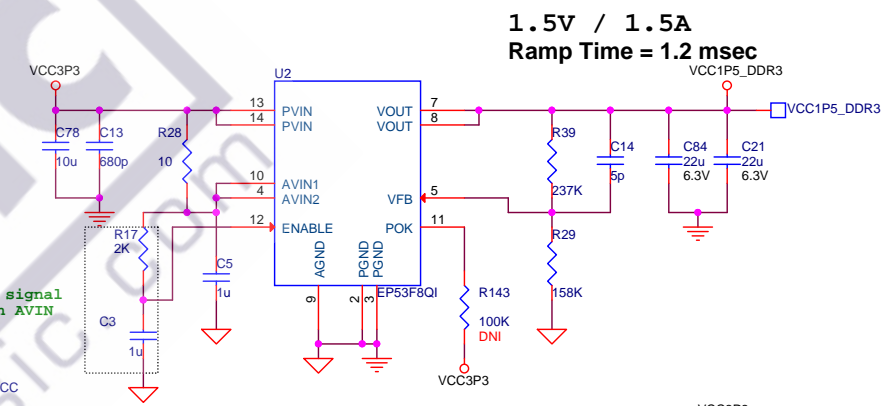
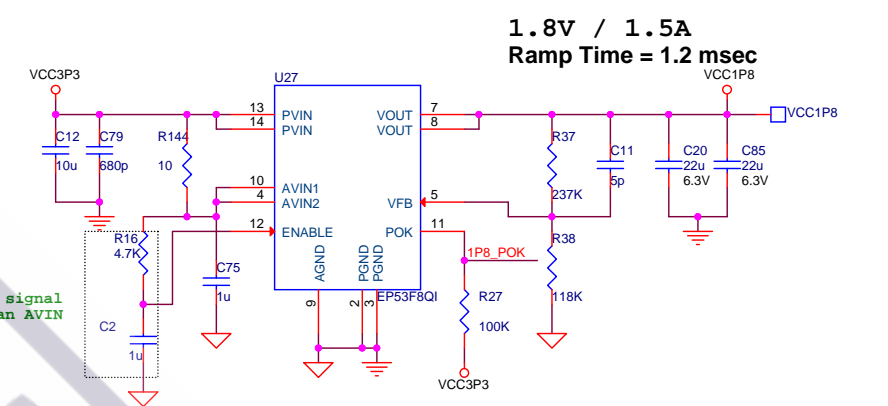
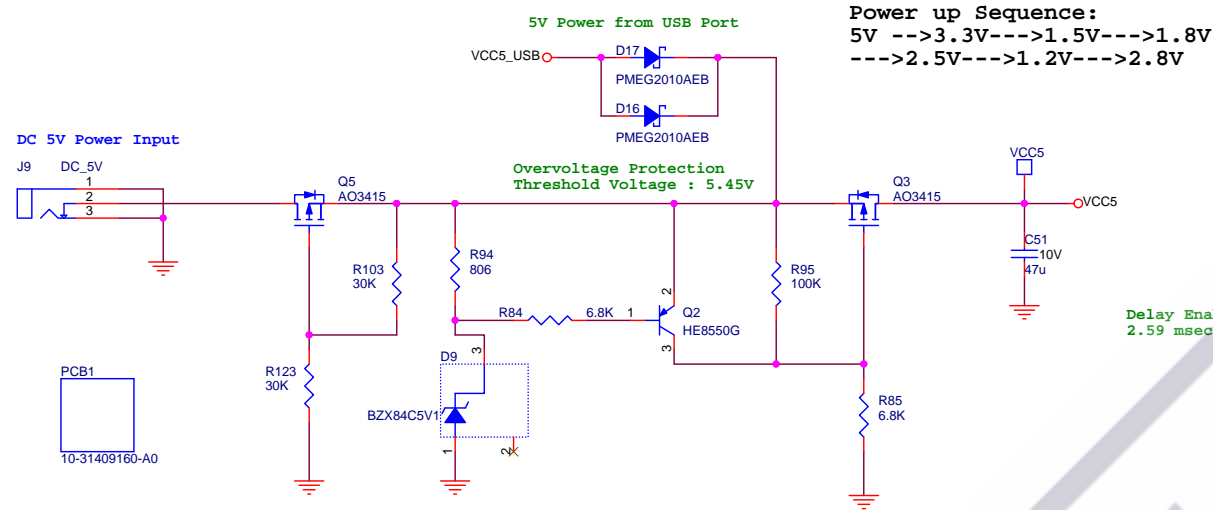
or place some other ICs to Isolate it?

**Proximity/Ambient Light Sensor**



Copyright (c) 2014 by Terasis Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasis.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	Gesture, Humidity, Temperature Sensors	C
Date:	Wednesday, March 11, 2015	Sheet 22 of 25

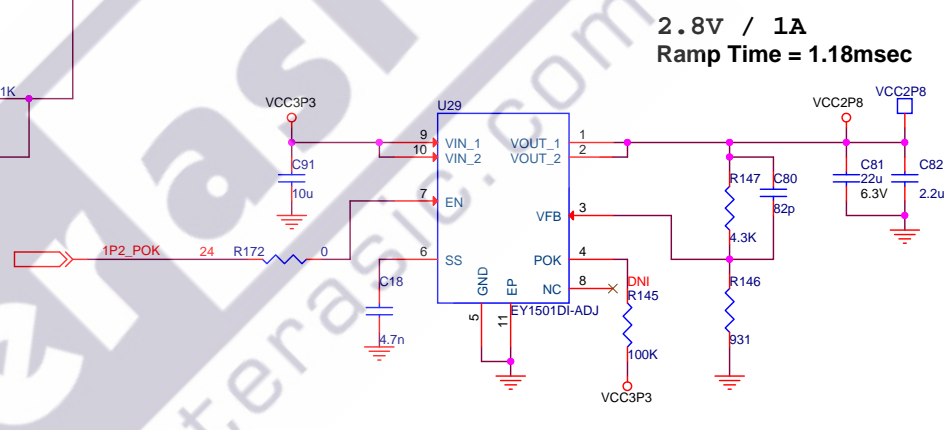
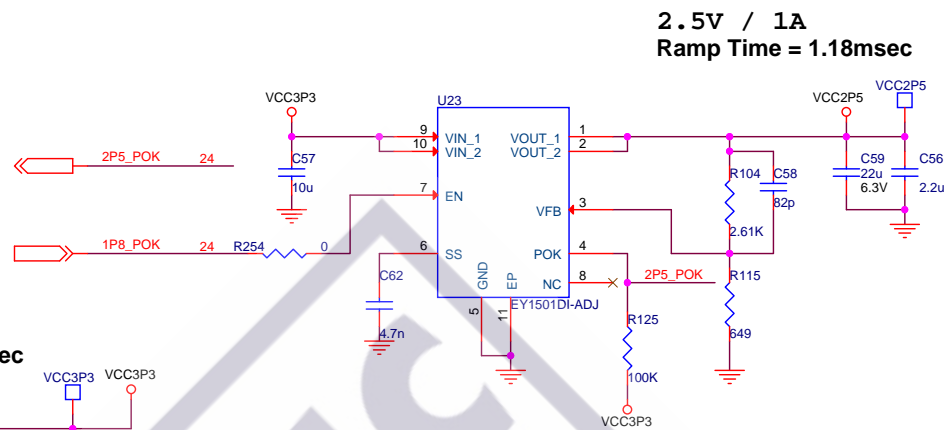
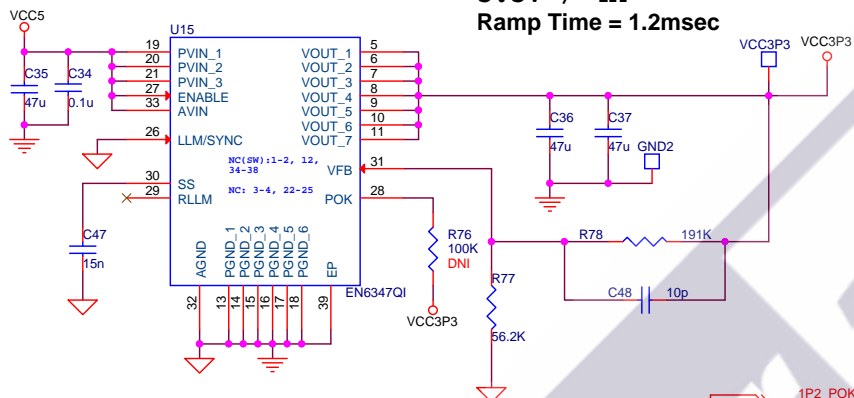





Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
<b>DECA</b>	
Size	Document Number
B	Power - 1.2V, 1.5V, 1.8V, 5V, Power Monitor
Date:	Wednesday, March 11, 2015
Sheet	24 of 25
Rev	C



Power up Sequence:  
 5V --->3.3V--->1.5V--->1.8V  
 --->2.5V--->1.2V--->2.8V



 Copyright (c) 2014 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
<b>DECA</b>		
Size	Document Number	Rev
B	Power - 2.5V, 2.8V, 3.3V	C
Date:	Wednesday, March 11, 2015	Sheet 25 of 25